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# Maximizing the Power of ARM® with DSP

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## Introduction

Texas Instruments' (TI) Integra™ DSP+ARM devices combine a digital signal processor (DSP) and an ARM® processor, enabling developers to create applications best suited for executing a combination of signal processing tasks and microprocessor (MPU) tasks. This paper reviews the benefits of combining ARM processing with DSP processing in a single chip, including increased real-time performance, improved system flexibility and reduced system cost and power. Integra DSP+ARM processors are useful for applications such as power protection systems, industrial control, machine vision and tracking and control. An argument for combining the power of the DSP with the general-purpose ARM processor is presented with data gathered from TI's OMAP-L13x and C6A816x Integra DSP+ARM processors demonstrating the benefit of running signal processing, math and image analysis algorithms on a DSP rather than an ARM processor. Example systems and the potential cost savings that can be achieved with DSP+ARM processors are also presented. Finally, an overview of the tools provided by TI to help ARM developers leverage the processing power of the DSP with minimal alterations to their application is given.

## Need for Heterogeneous Multi-Core Processors

In 2005, Herb Sutter famously predicted that the free lunch of ever-increasing processing performance was over (see <http://www.drdoobs.com/architecture-and-design/184405990>). Events since that time have confirmed his analysis. While transistor counts in processors have continued ever higher, core clock rates have stagnated and improvements in performance per Watt have dropped. The result has been chip architects putting the increasing transistor count to new uses, including larger on-chip memories and caches. More importantly, they have moved to add additional processing elements to their designs. We are now firmly in the era of multi-core computing.

Multi-core system-on-chip (SoC) design can be either homogeneous, with two or more of the same cores, or heterogeneous, with two or more different cores. Conceivably, the homogeneous design should be easier to work with as all cores share the same instruction set. For certain parallel tasks suited to that architecture, this is a good thing. However, more and more often our computing devices are being asked to simultaneously do very different things, many of which a general-purpose processor architecture is not particularly optimized for (hence the term "general purpose").

In these circumstances, the heterogeneous design begins to make sense: the architecture best suited for particular types of computation can be leveraged to most efficiently carry out a task. This should not be surprising, as the history of computing and digital semiconductors show. An example is graphics processing units (GPUs), which were created to handle 2-D and 3-D operations required by graphical user interfaces (GUIs) and games. Once a distinct part of every computer, the functionality of these chips is now moving back onto the silicon of the main CPU of desktop systems (see <http://www.amd.com/us/press-releases/Pages/amd-demonstrates-2010june02.aspx>). Such a move was made some time ago in certain embedded systems (like smartphones), for which space and power are at a premium. In short, programmable heterogeneous multi-core chips are here now and will continue to proliferate far into the future because of one simple fact – there is no "one-size fits all" computing architecture.

**Integra™:  
One of These Cores  
is Not Like the Other**

As a worldwide leader in digital signal processing and semiconductor manufacturing, TI has created silicon solutions combining the power of the DSP with the general-purpose capabilities of the ARM® architecture. Integra DSP+ARM processors consist of a DSP core and an ARM core. Integra combines the networking, file management and user interface features of an ARM processor running operating systems (OS) such as Linux™, Microsoft® Windows® Embedded CE and Android™, with the real-time, intensive signal-processing power of the DSP. Applications previously utilizing a multi-chip solution consisting of a separate DSP (or even multiple DSPs) and an MPU benefit greatly from this SoC design, resulting in reduced costs, complexity and power consumption.

Each current member of the Integra family integrates TI's TMS320C674x floating- and fixed-point DSP, together with an ARM MPU and a rich set of peripherals. Integra DSP+ARM processors offer designers an increase in overall system performance by utilizing the DSP for what it does best (real-time, intensive signal processing) and utilizing the ARM for what it does best (system control and applications processing). Additionally, the diverse on-chip peripherals provide network connectivity (EMAC and USB 2.0), high speed memory interfaces (DDR2 and/or DDR3) and standard bus interfaces (PCI Express 2.0, I<sup>2</sup>C, UART, etc.). This integration can result in a dramatic bill of materials (BOM) cost reduction as will be illustrated later. As an example, consider the block diagram of the C6A8168/67 Integra DSP+ARM processor shown in Figure 1.

**The Case for DSP**

The OMAP-L13x and the C6A816x Integra DSP+ARM processors from TI showcase the value and performance lines of the Integra family respectively. The OMAP-L13x Integra DSP+ARM processors include a C674x floating- and fixed-point DSP and an ARM926EJ-S™ each capable of running up to 456 MHz, while the C6A816x Integra DSP+ARM processors include a C674x floating- and fixed-point DSP and a higher performance ARM Cortex™-A8 with speeds up to 1.5 GHz.

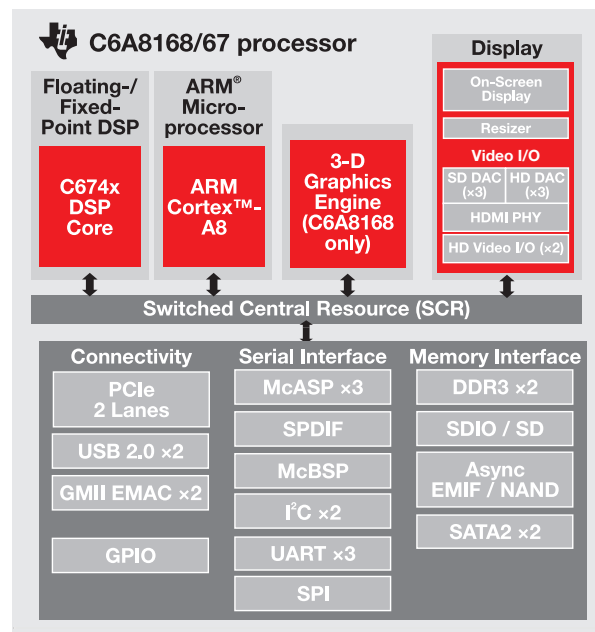


Figure 1. Block diagram of C6A8168/67 SoC.

## FFT performance

The Fast Fourier Transform (FFT) operation is likely the most common signal-processing algorithm in use today. The FFT is a computationally optimal way of converting time-domain signals to the frequency-domain, where analysis and processing are often more useful. Since this operation is so common in a diverse range of signal-processing algorithms, a performance comparison between the ARM® and DSP could be considered indicative of overall signal processing performance.

**Table 1. FFT cycle count comparison**

	C674x DSP	ARM Cortex™-A8
256-point 16-bit fixed-point complex FFT	934 clock cycles	1900 clock cycles

As Table 1 shows, the DSP can offer roughly twice the performance of the ARM for calculating a 256-point fixed-point complex FFT.

## Kernel benchmarks

As another example of the boost in performance obtained by running computationally intensive code on the DSP as opposed to the ARM, consider the case of image and signal processing functions shown in Table 2 below. In this case, a C6A816x Integra DSP+ARM processor is used to run these algorithms both on the ARM Cortex-A8 and on the C674x DSP. The DSP is running optimized code at 800 MHz and the ARM Cortex-A8 is running equivalent natural C code at 1 GHz. In all cases, the DSP is able to provide a performance boost over the ARM even with the ARM being clocked 25 percent faster. Note that included in these numbers is the overhead in cycles incurred when the ARM Cortex-A8 makes procedure calls to these algorithms running on the C674x DSP.

**Table 2. Performance comparison between ARM Cortex-A8 and C674x floating-/fixed-point DSP on fixed-point functions**

Image processing functions	Image Size	C674x Timing (µs)	ARM Cortex-A8 with O3+NEON timing (µs)	C674x improvement over A8
8-bit histogram	640×480	1770	2258	21.67%
8-bit 3×3 median filter	640×480	3418	15136	77.41%
8-bit 3×3 signed image convolution	640×480	3387	25817	86.88%
8-bit 3×3 image correlation	640×480	7873	16327	51.77%
8-bit 3×3 Sobel edge detection	640×480	3296	7415	55.54%
8-bit YUV422ILE to YUV422pl conversion	800×600	9063	19592	53.74%
8-bit YUV422PL to RGB565 conversion	800×600	8606	12543	31.38%
8-bit image addition	640×480	2197	3082	28.71%

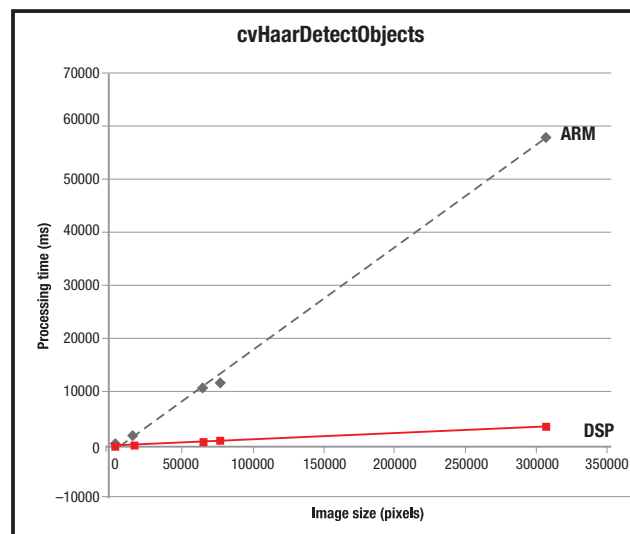
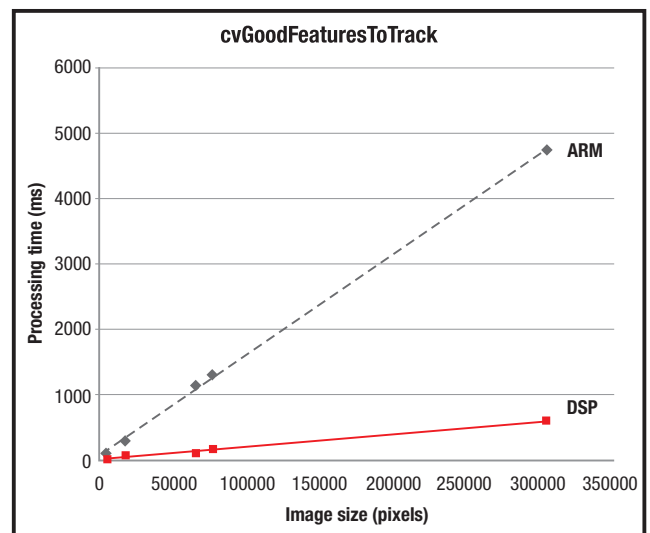
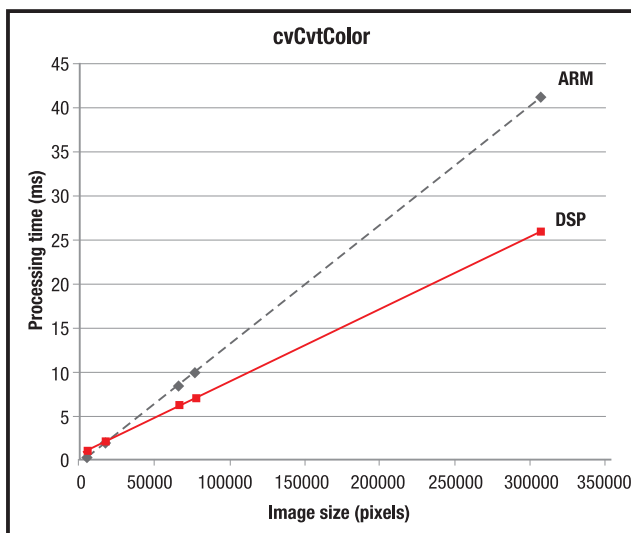
Signal processing	Size of Input	C674x Timing (µs)	ARM Cortex-A8 with O3+NEON timing (µs)	C674x improvement over A8
16-bit autocorrelation	256	549	3784	85.49%
16-bit matrix multiplication	64×64	641	1801	64.408%

The increased performance obtained from the DSP provides a compelling case for ARM® developers seeking higher system performance to consider using the DSP instead of upgrading their platform to a faster ARM core. Additionally, developers can also add more features to their application by freeing up processing power on the ARM core while using the DSP as a co-processor/accelerator to run computationally intensive algorithms.

### Application benchmarks

Clearly, raw computational kernel performance is important, but the code a typical user runs is not purely mathematical operations and signal-processing functions. Yet more complex application-level application programming interfaces (APIs) can also exhibit a significant boost when run on the DSP instead of on the ARM core.

Consider the performance of the `cvCvtColor`, `cvGoodFeaturesToTrack` and `cvHaarDetectObjects` functions from the Open Source Computer Vision (OpenCV) library when run on the C674x floating- and fixed-point

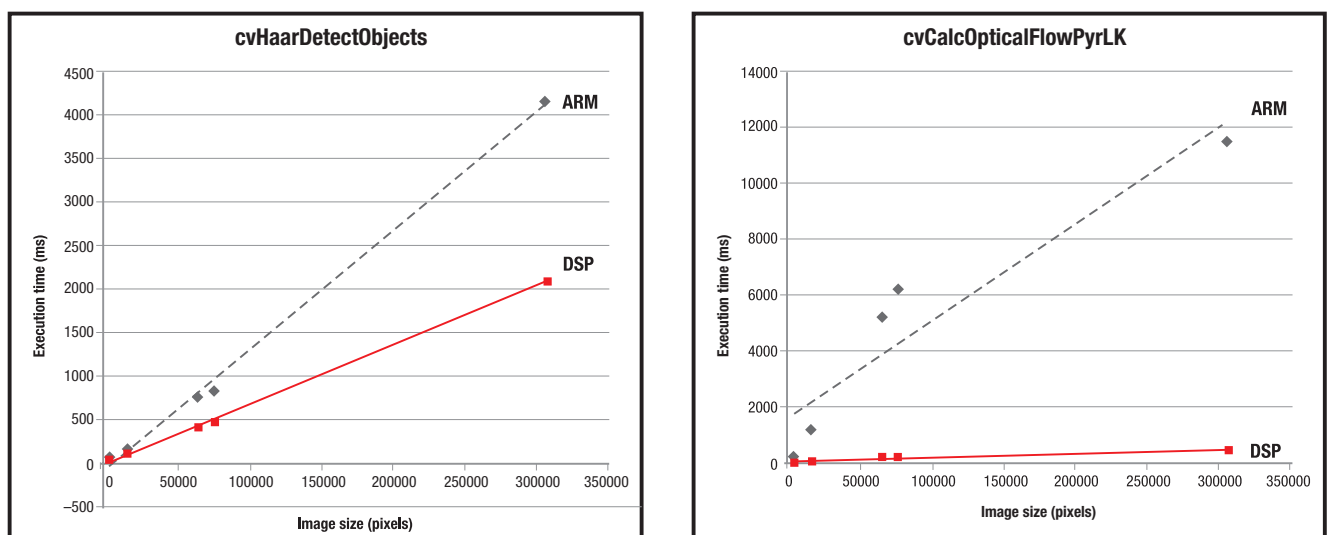


Figures 2a–2c. Performance comparison of `cvCvtColor`, `cvGoodFeaturesToTrack` and `cvHaarDetectObjects` when run on C674x DSP and ARM926EJ-S at 456 MHz.

DSP and the ARM926EJ-S™ of an OMAP-L138 Integra™ DSP+ARM® processor. Note that in Figures 2a–2c on the previous page, the APIs are being called from an ARM application running under the Linux™ operating system, but the execution of the APIs takes place on the DSP. Therefore, the numbers given for the DSP include overhead composed of operations such as address translations, cache invalidations and the function calls themselves. Despite this overhead, Figures 2a through 2c show that when the ARM uses the DSP to execute these functions, they execute much faster than when they are run directly on the ARM, especially as the size of the data set is increased and the overhead becomes a smaller fraction of the execution time. Note that in all three cases, the ARM926EJ-S and C674x DSP run at 456 MHz (code and data located in external memory, ARM and DSP data and program caches enabled). Also note the algorithms contain a mixture of floating- and fixed-point calculations and the ARM926EJ-S does not natively support floating-point instructions. This is another reason why the C674x DSP has faster execution time.

Now consider the performance of several OpenCV APIs when run on the DSP and ARM cores of the C6A816x Integra DSP+ARM processor. As Figures 3a and 3b show, even on a device with a higher-performance ARM (the ARM Cortex™-A8 with NEON instead of the ARM9™) which natively supports floating point in hardware, the DSP can still offer significant performance improvements. Again, the numbers for the DSP include the overhead of calling the DSP from the ARM core. The data for these figures come from an ARM Cortex-A8 at 1 GHz and a C674x DSP at 800 MHz (code and data located in external memory, ARM and DSP data and program caches enabled).

A short description of the OpenCV APIs used in the graphs of Figures 2 and 3 is given in Table 3 on the following page.



Figures 3a–3b. Performance comparison of `cvHaarDetectObjects` and `cvCalcOpticalFlowPyrLK` when run on 800-MHz C674x DSP and 1-GHz ARM Cortex-A8.

**Table 3. Description of OpenCV APIs**

cvCvtColor	Converts image from one color space to another.
cvGoodFeaturesToTrack	Finds corners with big eigenvalues in the image.
cvHaarDetectObjects	Finds rectangular regions in image likely to contain objects indicated by cascade.
cvCalcOpticalFlowPyrLK	Calculates optical flow for a sparse feature set using iterative Lucas-Kanade method in pyramids.

**System Integration Examples**

**Integra™ DSP+ARM® Value Line**

The OMAP-L13x generation of Integra DSP+ARM devices is used in a wide range of applications today. As previously mentioned, these devices include a C674x floating- and fixed-point DSP and an ARM926EJ-S™ core with speeds up to 456 MHz as well as multiple connectivity options, including USB, MMC/SD, serial ATA and an LCD controller. One particular application is protection systems that monitor and analyze power networks in real time and advise human operators of network abnormalities that can potentially lead to failure.

Power-protection systems must collect and analyze large amounts of widely varying analog data in real time. Data analysis requires a powerful DSP core. Some of the capabilities required include harmonic analysis, measuring the static differences for voltage and current, peak voltage/current fluctuation, power factor calculation and phase asymmetry detection. Aside from the signal-processing requirements, power-protection systems must also manage input/output (I/O) activities and control a GUI. Previous systems utilized a dual-chip approach to meet these two requirements.

The dual-core architecture of the OMAP-L13x Integra DSP+ARM processor lends itself naturally to the requirements of power-protection systems. The ARM on the device handles non-real-time tasks, while the DSP takes care of the data processing. Figure 4 shows a block diagram of a power-protection system using an OMAP-L138 Integra DSP+ARM processor. Note the \$12–14 savings in system cost.

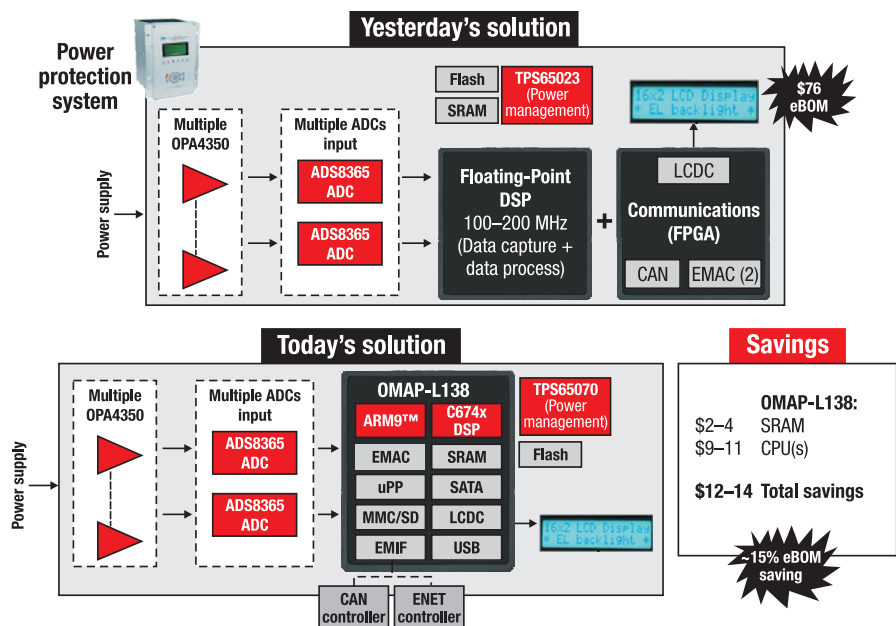


Figure 4: Before and after designs for a power-protection system using the OMAP-L138 Integra DSP+ARM processor.

Power-protection systems must run continuously for 10 years in an industrial environment in which operating temperatures are high. This makes power consumption critically important. The OMAP-L138 Integra™ DSP+ARM® processor keeps both active and static power consumption at very low levels. The SoC offers the following power saving techniques:

- Dynamic voltage and frequency scaling (DVFS): Frequency and voltage can be scaled just enough by the application to meet the real-time requirement. This reduces the percentage of CPU idle time and saves energy.
- Clock gating: Turning off the clock of the unused peripherals to save power from unnecessary clock toggling.
- For certain high-power components on the chip, e.g., USB PHY, the SoC can be carefully designed to allow cutting off the power supply to the component.

### **Integra performance line**

The new Integra DSP+ARM performance processors, such as those of the C6A816x generation, have application in a variety of more performance-intensive computing systems. As stated earlier, these SoC devices include a C674x floating- and fixed-point DSP and an ARM Cortex-A8 with speeds up to 1.5 GHz. To match these higher-performance processors, the integrated peripheral set includes high-speed connectivity options such as PCI Express (PCIe) 2.0 and dual gigabit Ethernet MACs. These devices can also include advanced display engines and 3-D graphics accelerators for creating impressive and intuitive visual interfaces. One application that can see significant potential benefit from the use of such a highly integrated and powerful device is machine vision. In particular, let us consider equipment that is used for automated visual inspection of products on a production line.

Machine vision systems deal with lots of high-resolution images, which translate to massive amounts of data per second. A high-performance processor is required to analyze these images in real time, a requirement satisfied by the 1.5-GHz floating- and fixed-point DSP. To keep the processor fed with data and to communicate results to the outside world, high-bandwidth I/O interfaces are also required. Two 32-bit DDR3 memory interfaces operating at up to 1600 MHz, along with the collection of high-speed interfaces mentioned previously (such as the two gigabit Ethernet MACs), provide the required bandwidth to control multiple operations going on within the machine vision system and optionally send raw images and inspection results back to a remote operator.

The new C6A816x Integra DSP+ARM processors come with a library of imaging- and vision-analysis algorithms that have an OpenCV API and are accelerated on the integrated floating- and fixed-point DSP. This can allow machine vision software architects to use their existing applications and algorithms while utilizing the power of the DSP to increase the performance of their systems. Furthermore, machine vision algorithm developers typically write their prototype software on a PC in floating point. Having a high-performance floating-point DSP allows the algorithm designer to easily and quickly port their code from the desktop computer to an embedded environment. This also eases long-term maintenance and upgrade concerns, as the algorithm prototyped on the PC can be exactly the same as that running on the target embedded system.

Future system changes can be done without potentially lengthy and expensive conversions from floating to fixed point.

The heterogeneous dual-core architecture of the Integra DSP+ARM® meshes naturally to the requirements of machine vision system. The ARM on the SoC handles non-real-time tasks, while the DSP takes care of the data processing and analysis.

Figure 5 shows a block diagram of a machine-vision application, indicating how the one individual C6A816x Integra DSP+ARM processor can replace a discrete microprocessor, FPGA and DSP. Furthermore, the required memories associated with each of those components are also consolidated to a single set of chips. In total, nine distinct parts are converted to only three parts. This results in an approximate 50 percent cost savings going from a multi-chip solution to a solution powered by the C6A816x Integra DSP+ARM processor. The consolidation offered by TI's SoC can lead to smaller PCB requirements, which also can in turn enable smaller overall form factors. In addition, the system power requirements are potentially reduced, further lowering the system's total cost of ownership.

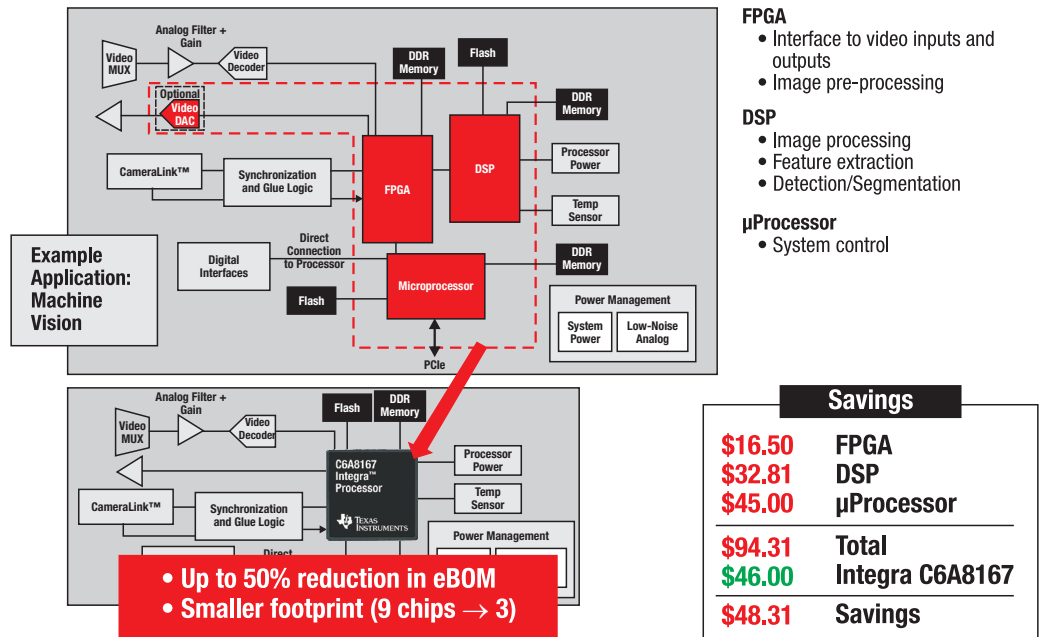


Figure 5. Before and after designs for a machine-vision application using the C6A8167 Integra DSP+ARM processor.

**Software Solutions: Tools for Code Construction**

It is clear that an Integra DSP+ARM processor, as a silicon solution, offers compelling value due to its high level of integration, including the DSP cores and general-purpose ARM architectures. However, tools must be available that enable programmers with different levels of DSP programming experience to tap into the computational power offered by such devices. Sutter's prediction that the "free lunch" was over is ultimately based on one unfortunate fact—multi-core programming is not as easy as single-core programming.

Developers face many challenges when working with heterogeneous cores, many of them related to software development: different code-generation tools, operating system differences and allocation of shared

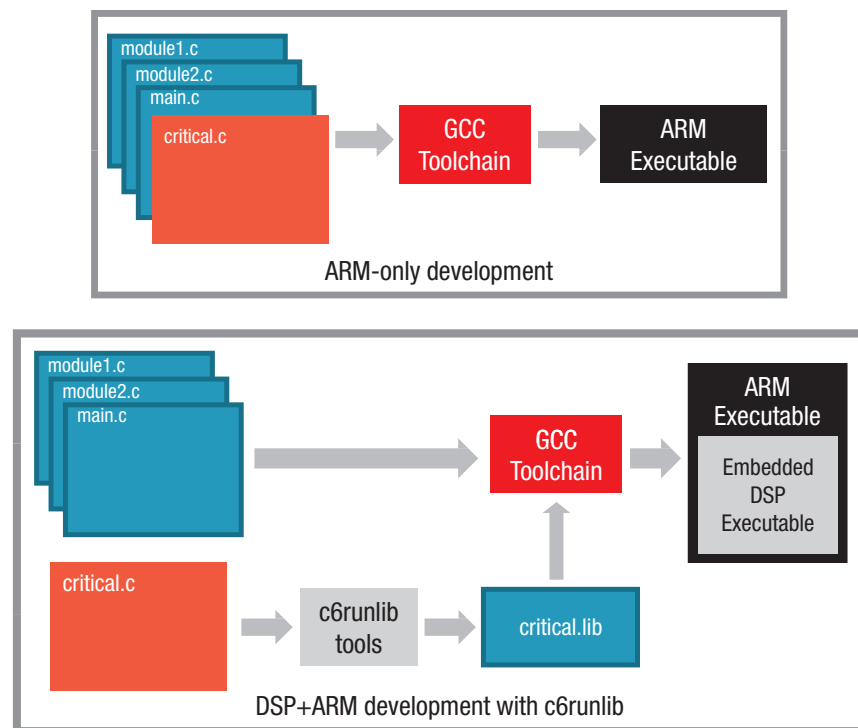
resources. Additionally, the learning curve for understanding and programming the DSP is often perceived as too steep to justify potential performance benefits. With this in mind, TI has a collection of tools intended to make DSP programming easier for different types of developers with different types of needs.

**Table 4. Tools for programming the DSP**

Embedded developers	Customer needs	Tool
ARM® developer	Leverage the DSP without specialized knowledge	C6EZRun
System developer	More ready-to-use DSP functionality with audio, video and voice codecs	C6EZAccel
Advanced user/Developer	Optimized libraries, real-time OS and development tools	Libraries SYS/BIOS SYS/LINK

### C6EZRun

The C6EZRun tool from TI allows ARM developers with little to no DSP programming experience to do two things: run an ARM application entirely on the DSP without changing their ARM code and create a library of ARM-callable functions that run on the DSP. The ability to run an ARM application directly on the DSP allows users to quickly profile their code on the DSP. Basic features such as C I/O are supported, so the DSP gains access to the ARM filesystem. No modification of the ARM code is required, and code can be compiled directly from a Linux shell. Furthermore, there is no need to learn any DSP architecture details.



*Figure 6. DSP library development with C6EZRun.*

The C6EZRun tool is ideally suited for accelerating existing ARM® applications by offloading critical or bottlenecked portions of the code to the DSP (consider the evidence the benchmarks provided earlier in this paper). Figure 6 on the previous page shows the process by which this can be done. As a test of this capability, the C6EZRun tool was used to move portions of a Qt GUI application from Nokia's Qt software development kit to the DSP. The application, which generated and displayed fractal images, executed 35 times faster when accelerated by the DSP on the OMAP-L138 Integra DSP+ARM SoC device. For more information on the C6EZRun tool, please refer to the [C6EZRun whitepaper](#).

### C6EZAccel

For system developers who may be looking to extract more performance from their Integra DSP+ARM device, the C6EZAccel tool provides a way to leverage math, image processing and digital-signal-processing libraries, all of which run on the DSP. C6EZAccel also provides a framework which system developers can use to add their proprietary algorithms. C6EZAccel makes available fully optimized, benchmarked and tested DSP libraries, allowing developers to easily take advantage of DSP features. Note that the ARM can continue to perform other tasks while the DSP runs C6EZAccel library functions.

Figure 7 below shows how the C6EZAccel tool fits into the software development framework used on TI's SoCs. As an example use of the C6EZAccel tool, the benchmarks given earlier in this paper to compare the ARM and DSP performance were run using the C6EZAccel tool. For more information on the C6EZAccel tool, please refer to the [C6EZAccel whitepaper](#).

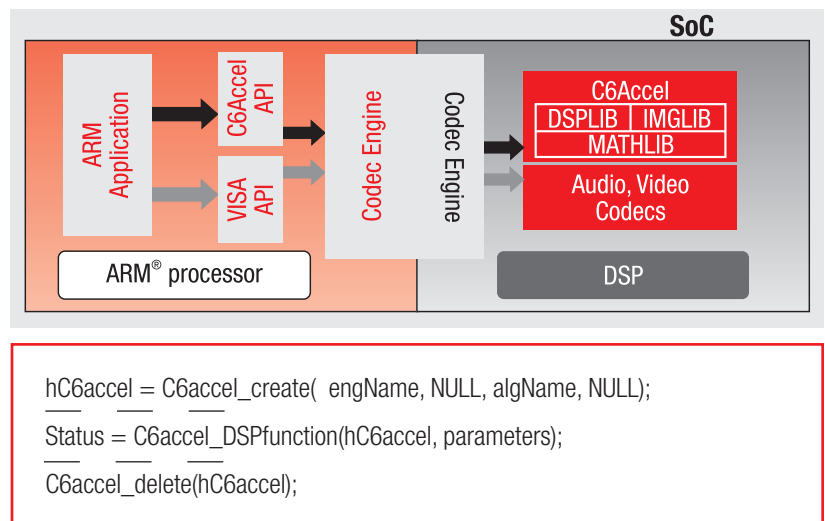


Figure 7. Block diagram of C6EZAccel software usage.

### Low-Level DSP Programming

Finally, for advanced users and developers that are looking to extract the maximum performance from their DSP+ARM SoC, DSP-optimized libraries, a real-time OS and a communication link to the ARM are absolutely required. For these types of developers, TI offers a range of software tools including:

- SYS/BIOS: a scalable real-time kernel, which provides preemptive multi-threading, hardware abstraction, real-time analysis and configuration tools
- Multiple DSP libraries: including floating- and fixed-point DSP libraries, an image-/video-processing library, a high-precision math library and a floating-point math library
- SYS/Link: a software link for inter-processor communication across the ARM®–DSP boundary.

### **Conclusion**

By combining a DSP and ARM® processor in a single package, the Integra™ DSP+ARM platform of processors brings many benefits to system design, including increased real-time performance, improved system flexibility and reduced system cost and power. The on-chip peripherals included on Integra provide network connectivity (EMAC and USB 2.0), high-speed memory interfaces and standard bus interfaces (PCI Express 2.0, I<sup>2</sup>C, UART, etc.) which further add to the system performance and further reduce system cost. As the benchmarks have shown, the real-time response and floating-/fixed-point numerical performance of the DSP provides a natural advantage to ARM processors when it comes to running computationally intensive algorithms. The example systems discussed in this paper show the potential cost savings that can be achieved with Integra DSP+ARM processors, as both chip count and board area are reduced. To help ARM developers leverage the processing potential of the DSP, TI provides a number of free tools that allow the ARM developer to remain in the Linux™ development environment without the need to change his/her ARM application code. The Integra platform means a balanced approach to system design, from silicon to software.

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DLP® Products	<a href="http://www.dlp.com">www.dlp.com</a>	Communications and Telecom	<a href="http://www.ti.com/communications">www.ti.com/communications</a>
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