



# LCD Connectivity

Document Reference  
Document Issue Level

LCD Connectivity  
1.0

**Blue Chip Technology Ltd.**  
**Chowley Oak**  
**Tattenhall**  
**Chester**  
**CH3 9EX**  
**U.K.**

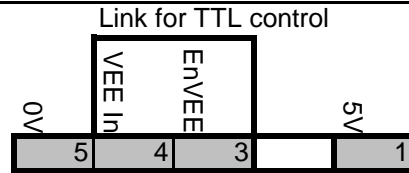
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**[www.bluechiptechnology.co.uk](http://www.bluechiptechnology.co.uk)**

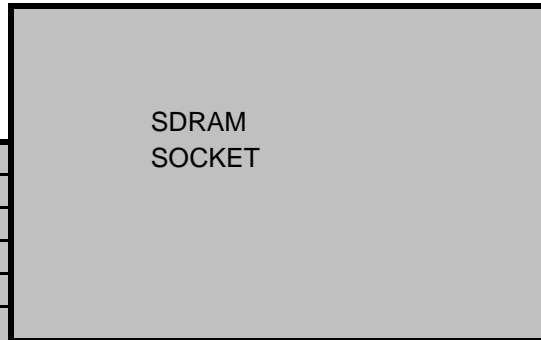
TFT 18 bit, 18+18

See "Board Layout"

P5



5V	3	
VCC	2	VCC source
3V3	1	J2



VCC	1	2	VSYNC
SW12V	3	4	GND
VEEIn	5	6	HSYNC
SWVCC	7	8	GND
SWVCC	9	10	ENABKL
DCLK	11	12	GND
LCLK/LP	13	14	
MOD/DE	15	16	GND
FLM	17	18	GND
RED5	19	20	GND
RED4	21	22	(S2)
RED3	23	24	GND
RED2	25	26	(S1)
GREEN5	27	28	GND
GREEN4	29	30	
GREEN3	31	32	GND
GREEN2	33	34	
BLUE5	35	36	GND
BLUE4	37	38	
BLUE3	39	40	GND
BLUE2	41	42	
RED1	43	44	GND
RED0	45	46	BLUE0
GREEN1	47	48	GND
GREEN0	49	50	BLUE1

P5 EnVEE is a TTL o/p from Micron  
VEEIn is a wire to P6

Link P5 pins 3/4 to pass TTL signal to panel for VEE sequencing

VCC is supplied from J2  
SWVCC is a sequenced supply from J2  
SW12V is sequenced 12V

Some panels require specific supply sequencing

P6 2mm shell 2x25

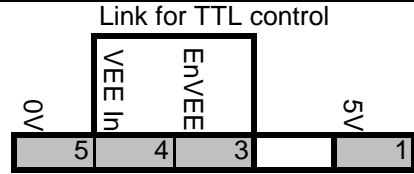
S1=CLOCK FOR ODD PIXEL  
S2=CLOCK FOR EVEN PIXEL

Sequence	ON	SWVCC	Signals	ENVEE	ENABKL/SW12V	
	OFF	ENABKL/SW12V	ENVEE	Signals	SWVCC	

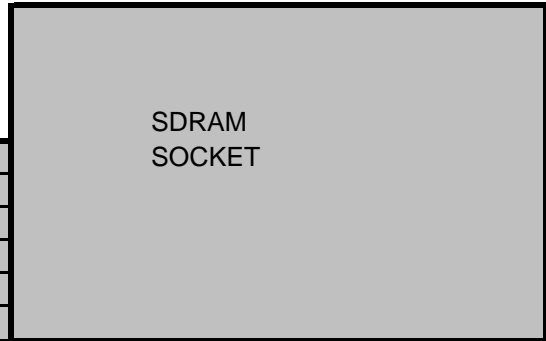
TFT 12

See "Board Layout"

P5



5V	3	
VCC	2	VCC source
3V3	1	J2



VCC	1	2	VSYNC
SW12V	3	4	GND
VEEIn	5	6	HSYNC
SWVCC	7	8	GND
SWVCC	9	10	ENABKL
DCLK	11	12	GND
LCLK/LP	13	14	
MOD/DE	15	16	GND
FLM	17	18	GND
RED3	19	20	GND
RED2	21	22	S2
RED1	23	24	GND
RED0	25	26	S1
GREEN3	27	28	GND
GREEN2	29	30	
GREEN1	31	32	GND
GREEN0	33	34	
BLUE3	35	36	GND
BLUE2	37	38	
BLUE1	39	40	GND
BLUE0	41	42	
	43	44	GND
	45	46	
	47	48	GND
	49	50	

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P6 2mm shell 2x25

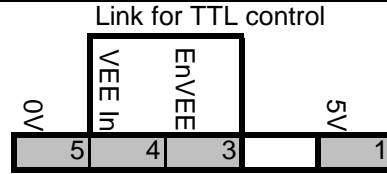
S1=CLOCK FOR ODD PIXEL  
S2=CLOCK FOR EVEN PIXEL

Sequence	ON	SWVCC	Signals	ENVEE	ENABKL/SW12V	
	OFF	ENABKL/SW12V	ENVEE	Signals	SWVCC	

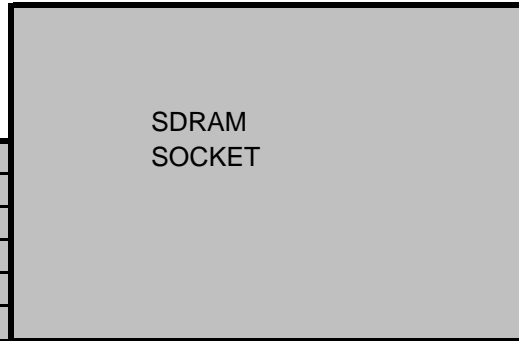
TFT 12, 12 + 12

See "Board Layout"

P5



5V	3	
VCC	2	VCC source
3V3	1	J2



VCC	1	2	VSYNC
SW12V	3	4	GND
VEEIn	5	6	HSYNC
SWVCC	7	8	GND
SWVCC	9	10	ENABKL
DCLK	11	12	GND
LCLK/LP	13	14	
MOD/DE	15	16	GND
FLM	17	18	GND
RO3	19	20	GND
RO2	21	22	BE0
RO1	23	24	GND
RO0	25	26	BE1
GO3	27	28	GND
GO2	29	30	BE2
GO1	31	32	GND
GO0	33	34	BE3
BO3	35	36	GND
BO2	37	38	GE0
BO1	39	40	GND
BO0	41	42	GE1
RE3	43	44	GND
RE2	45	46	GE2
RE1	47	48	GND
RE0	49	50	GE3

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P6 2mm shell 2x25

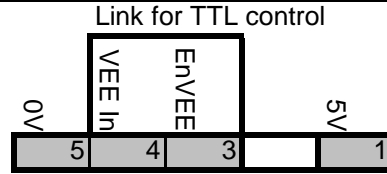
E=EVEN PIXEL  
O=ODD PIXEL

Sequence	ON	SWVCC	Signals	ENVEE	ENABKL/SW12V
	OFF	ENABKL/SW12V	ENVEE	Signals	SWVCC

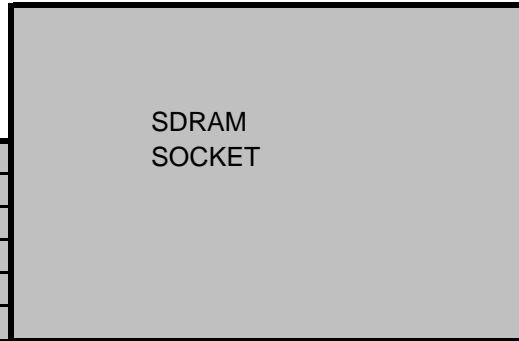
DSTN 16bit

See "Board Layout"

P5



5V	3	
VCC	2	VCC source
3V3	1	J2



VCC	1	2	VSYNC
SW12V	3	4	GND
VEEIn	5	6	HSYNC
SWVCC	7	8	GND
SWVCC	9	10	ENABKL
DCLK	11	12	GND
LCLK/LP	13	14	
MOD/DE	15	16	GND
FLM	17	18	GND
LD0	19	20	GND
LD1	21	22	
LD2	23	24	GND
LD3	25	26	
LD4	27	28	GND
LD5	29	30	
LD6	31	32	GND
LD7	33	34	
UD0	35	36	GND
UD1	37	38	
UD2	39	40	GND
UD3	41	42	
UD4	43	44	GND
UD5	45	46	
UD6	47	48	GND
UD7	49	50	

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P6 2mm shell 2x25

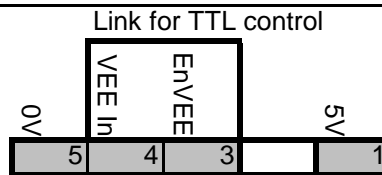
U=UPPER  
L=LOWER

Sequence	ON	SWVCC	Signals	ENVEE	ENABKL/SW12V	
	OFF	ENABKL/SW12V	ENVEE	Signals	SWVCC	

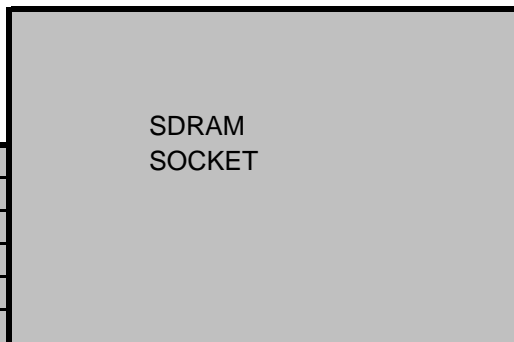
DSTN 24bit

See "Board Layout"

P5



5V	3	
VCC	2	VCC source
3V3	1	J2



VCC	1	2	VSYNC
SW12V	3	4	GND
VEEIn	5	6	HSYNC
SWVCC	7	8	GND
SWVCC	9	10	ENABKL
DCLK	11	12	GND
LCLK/LP	13	14	
MOD/DE	15	16	GND
FLM	17	18	GND
LD0	19	20	GND
LD1	21	22	UD11
LD2	23	24	GND
LD3	25	26	UD10
LD4	27	28	GND
LD5	29	30	UD9
LD6	31	32	GND
LD7	33	34	UD8
LD8	35	36	GND
LD9	37	38	UD7
LD10	39	40	GND
LD11	41	42	UD6
UD0	43	44	GND
UD1	45	46	UD5
UD2	47	48	GND
UD3	49	50	UD4

P5 EnVEE is a TTL o/p from Micron  
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P6 2mm shell 2x25

U=UPPER  
L=LOWER

Sequence	ON	SWVCC	Signals	ENVEE	ENABKL/SW12V	
	OFF	ENABKL/SW12V		ENVEE	Signals	SWVCC