BCT-ETX-CN700

ETX Format Single Board Computer
User Guide

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Contents

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CE
This product meets the essential protection requirements of the European EMC Directive (2004/108/EC) and the Low Voltage Directive (2006/95/EC), and is eligible to bear the CE mark.

Warning

This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC
NOTE:
This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

WARNING:

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

Safety Warning for North America

If the power lead (cord) is not supplied with the computer, select a power lead according to your local electrical regulations. In the USA use a 'UL listed' lead. In Canada use a CSA approved or 'cUL listed' lead.

Si le cordon secteur n'est pas livré avec l'ordinateur, utiliser un cordon secteur en accord avec votre code electrique nationale. En l'Etat Unis utiliser un cordon secteur 'UL listed'. En Canada utiliser un cordon secteur certifié CSA, ou 'cUL listed'.

Manual Organisation

This manual describes in detail the ETX CN700 range of Single Board Computers.

We have tried to include as much information as possible but we have not duplicated information that is provided in the standard IBM Technical References, unless it proved to be necessary to aid in the understanding of the product.

The manual is sectioned as follows:

Introduction;
Overview, listing the unit's features and specification;
Installation, including what software to install
Layout, showing where the various connectors are located, and their pin-out details;
How to upgrade the system;
Bios Setup
Connector Details
Design Considerations
Maintenance details

We strongly recommend that you study this manual carefully before attempting to interface with board or change the standard configurations. Whilst all the necessary information is available in this manual we would recommend that unless you are confident, you contact your supplier for guidance.

IT IS PARTICULARLY IMPORTANT THAT YOU READ THE SECTION 'PRECAUTIONS' BEFORE HANDLING ANY COMPONENTS INSIDE THE UNIT.

If you have any suggestions or find any errors concerning this manual and want to inform us of these, please contact our Technical Services department with the relevant details.

Introduction

The Blue Chip Technology ETX CN700 complies with the embedded ETX standard Version 3.02 set of Bus interface signals and peripheral IO devices interfaces on a single card. The concept of ETX is to provide the user with a standard connector interface with fixed connector locations and predefined IO functions. This allows the user to concentrate their design efforts on the supporting base board for the target application. This modular approach provides a cost effective means of system upgrade and allows the user to easily validate a number of CPU board price/power/performance options.

Following on from the highly successful BCT-ETX-C3, the Blue Chip Technology ETX CN700 Single Board computer integrates the latest advances in processor, graphics, memory, and I/O technologies to provide not only an ideal platform for new embedded designs, but also a means of upgrading existing ETX based applications to take advantage of the latest technologies.

The board is available with CPU build options of Ultra Low Voltage VIA Eden 500Mhz, VIA C7 nanobga2 1GHz and the VIA C7 nanobga2 1.5GHz processors. On-board voltage regulator circuits provide the required voltages for the processor from the incoming 5 volt power supply. The 500MHz version is targeted at lower cost, power conscious, performance driven applications. Where reduced power is less of a requirement then the 1GHz and 1.5GHz versions offer a higher performance solution.

Further additions to the range are the VIA Nano-E series processors which both support 64bit OS's: the Low Power 800MHz U3400, and the 1.3GHz U3100

The processor maintains full backward compatibility with the 8086, 80286, i386™ and Intel486™ processors. It supports both read and write burst mode bus cycles, and includes separate on-chip code and data caches which employ a write-back policy. Cache is integrated within the CPU and operates at the full CPU frequency giving excellent performance. On the Eden/C7 CPU's, cache size is 128K L1 and 128K L2, while on the Nano, cache size is 64KB (data) +64KB (instruction) L1 and 1024KB L2. Also integrated into the processor is an advanced numeric co-processor which significantly increases the speed of floating point operations, whilst maintaining backward compatibility with Intel486™ math co-processor and complying with ANSI/IEEE standard 754-1985.

The memory interface supports up to 1GB of DDR2 SDRAM, in a standard 200 pin SODIMM socket.

The ETX CN700 utilises the VIA CN700 Northbridge and VT8237R Pus Southbridge to integrate many peripherals. These include: VGA controller with CRT, LVDS and LCD interfaces, ATA-100 IDE interface, 10/100 Fast Ethernet controller, floppy disk interface, quad USB ports, dual serial ports, parallel port, real-time clock, keyboard and mouse (PS/2) controller, AC'97 audio interface. Connection to these functions is made through a standard set of ETX connectors onto a base board. The base board can then bring these signals to either Industry standard or customer specified connectors. The base board may be a custom design, developed for a specific application or a standard solution offered by Blue Chip Technology. The VT8237R also provides SATA interface which is accessed via two SATA connectors positioned on the ETX CN700 SBC in accordance with the ETX V3.02 specification.

The ETX CN700 also has an on board USB connector which is only available to allow access to custom form factor Flash drives. Note. This is not a standard USB port and will not work with non flash devices

The ETX-CN700 will drive up to four external PCI cards, all of which can perform Bus Mastering. Further IO expansion is available through the 16-bit ISA bus.

Specification

CPU	VIA ULV Eden 500MHz VIA C7 nanobga2 1GHz/1.5GHz VIA Nano-E nanobag2 800MHz/1.3GHz
Chipset:	VIA CN700 Northbridge VIA VT8237R Plus Southbridge
BIOS:	Phoenix BIOS, with Ethernet Boot ROM option
Memory:	512MB to 1GB PC2-4200/5300 DDR2 400/533 SDRAM using Horizontal 200 pin SODIMM, 1.8V operation. DDR2 667MHz can be used but will operate at 533MHz
Cache:	128KB L1 and 128KB L2 Cache is integrated into the CPU
Onboard Peripherals	
Graphics:	Integrated graphics controller based on the Unichrome Pro 3D/2D Graphics controller. CRT, 18bit TFT LCD and LVDS SVGA up to 1920 x 1440 resolution
Ethernet:	Integrated controller providing 10/100 Base-T Ethernet Boot ROM option within the BIOS setup for remote booting (PXE) ***Note: the host board must carry the magnetic for network isolation***
Storage:	Integrated into Southbridge, providing support for SATA 1 (dual ports dual connectors) and ATA 133/100/66/33 EIDE HDD (quad ports, dual connectors) 512MB I^2C EEPROM providing non-volatile storage
Audio:	Integrated AC97 controller, Line In/Out, Microphone In
Communications:	Quad USB ver 2 compliant Two 16C550 compatible serial ports ***Note: Host board must provide transceivers*** Parallel port giving SPP/EPP/ECP Floppy Interface supporting single 1.44MB drive ***Note: the floppy or parallel port operation is determined at boot time By strapping a pin on the host board. The devices are mutually exclusive*** PS/2 compatible keyboard and mouse port
Monitoring:	CPU Core thermal monitoring On board thermistor for system thermal monitoring CPU Core, 1.8V, 2.5V, 3.3V and 5V voltage monitors Hardware Watchdog timer with configurable timeout BIOS or Software enabled/disabled. The time out results in a System Reset
Miscellaneous:	PC standard Real time Clock is integrated into the Southbridge The battery has to be located on the host board. Speaker, Power/Reset switch, Hard Disk Activity LED, Suspend Switch and external Lithium coin cell are all supported but located on the Host board

Expansion Bus:	As per ETX Specification, 4 connectors X1-X4 Connector X1 provides PCI Bus, USB and Audio Connector X2 provides the ISA Bus Connector X3 provides the VGA, LCD, COM1/2, LPT1, FDD, Keyboard and Mouse Connector X4 provides the Ethernet (non-isolated), 2 x EIDE (4 drives) Utilities signals, power management and control Supports four standard 5V 32bit 33MHz PCI Slots, V2.2 compliant Supports three standard 16-bit ISA slots
Board Profile:	114 x 95 mm
Power:	5Volt only operation (5V ± 5%) On board regulation for CPU core, 3.3V
General Operating:	Storage Temperature: -20°C to +70°C Operating Temperature: 0°C to +60°C ***Note: faster CPU speeds will require active cooling to achieve Operating limit*** Relative humidity: 10 – 90% non-condensing
Operating System Support:	Datalight ROM-DOS and TCP/IP Sockets Windows CE 6.0 Windows XP Professional Windows XP Embedded Windows Vista Linux QNX
Compliance	EMC Directive 2004/108/EC Low Voltage Directive 2006/95/EC RoHS Compliant
Safety	Designed to meet EN 60950-1
EMC	EN55022 Class A EN55024

General Precautions

Your Single Board Computer is susceptible to damage by electrostatic discharges. In order to avoid damage, you should work at an anti-static bench and observe normal anti-static precautions. Wear an anti-static wrist strap connected to an earth point *before* opening any packaging.

Where a wrist strap is not available, discharge any static charge you may have built-up by touching an earth point. Avoid any further movement that could build up another static charge. Touch an earth point from time to time to avoid further build-up, and remove the items from their anti-static bags only when required

PS/2 Devices

It is important that PS/2 devices (mouse and keyboard) are not connected or disconnected with the unit powered on. Damage or data corruption may occur if this precaution is not observed.

Electro-Static Discharges

If you are going to open up the unit, it is important to realise that the devices on the cards within this unit can be damaged by static electricity. Bear in mind that the damage caused by static electricity may vary from total destruction to partial damage, which may not be immediately obvious. This could have an effect on the product's reliability and warranty. Before opening the chassis, ensure that you take necessary static precautions. Ideally you should work at an anti-static bench and wear an approved wrist strap or if that is not possible, touch a suitable ground to discharge any static build up before touching the electronics. This should be repeated if the handling continues for any length of time.

If it is necessary to remove a board or electronic assembly, place it into an anti-static bag. This will prevent any static electricity build up damaging the board. Metallised bags are preferred. Do not use black anti-static bags for any item containing a battery because these tend to be conductive and will discharge the battery.

On-Board Battery

The ETX-CN700 board is does not have an on-board Lithium cell connected, however the base board to which it connects may be equipped with a cell. Great care should be taken with this type of battery. If the battery is mistreated in any way there is a very real possibility of fire, explosion, and personal harm. Under NO circumstances should it be short-circuited, exposed to temperatures in excess of 100°C or burnt, immersed in water, recharged or disassembled.

Expired batteries remain hazardous and must be disposed of in a safe manner, according to local regulations.

Le panneau de processeur est équipé d’une batterie de lithium. Le grand soin devrait être pris avec ce type de batterie. Si la batterie est mistreated il y a de dans de toute façon un possibility très vrai du feu, d’expolosion et de mal personnel. Dans au cunes circonstances il est sous peu circuité, exposé aux températures au dessus de 100 degrés de centrigrade ou brûlé, immergé dans l’eau, rechargée ou dissassambled.

Les batteries expirées restent dazaedous et doivent être reejetées d’une façon sûre, selon des règlements locaux.

BIOS & CMOS Memory

Please be aware that with personal computer products, it is possible to create configurations within the BIOS make booting impossible. Unlike most personal computer products, the ETX-CN700 stores the BIOS settings in Flash memory rather than CMOS which allows these settings to be remembered even if there is no battery present.

If settings are used which make the ETX-CN700 unstable, then clearing the CMOS as in other personal computers to return to defaults will not work. The only way to reset default BIOS settings is to enter BIOS at boot time and Load Default Settings.

WARNING: If you are uncertain as to consequences of making specific changes to BIOS settings, then consult Blue Chip Technology Technical Support for advice

Electromagnetic Compatibility

This product has been assessed operating in representative, standard configurations. As with any PC product, however, final installation & configuration can vary significantly, and so the following guidelines are offered to help ensure that compatibility is maintained.

- All components added to a system should either carry appropriate equivalent levels of compliance, or be tested for compliance as part of the final system, and should be installed in accordance with supplier recommendations.
- The external enclosure should be securely fastened (with standard lids and covers in place) to ensure good metal-to-metal contact around the internal electronics
- Any metal back plate must be securely screwed to the chassis of the computer to ensure good metal-to-metal (i.e. earth) contact.
- Metal, screened, connector bodies should be securely connected to the enclosure.
- The external cabling to boards causes most EMC problems. It is recommended that any external cabling to the board be totally screened, and that the screen of the cable connects to the metal end bracket of the board or the enclosure and hence to earth. Round, screened cables with a braided wire screen are used in preference to those with a foil screen and drain wire. Wherever possible, use metal connector shells that connect around the full circumference of the cable screen: they are far superior to those that earth the screen by a simple “pig-tail”.
- The keyboard and mouse will play an important part in the compatibility of the processor card since they are ports into the board. Similarly, they will affect the compatibility of the complete system. Fully compatible peripherals must be used otherwise the complete system could be degraded. They may radiate or behave as if keys/buttons are pressed when subject to interference. Under these circumstances it may be beneficial to add a ferrite clamp on the leads as close as possible to the connector. A suitable type is the Chomerics type H8FE-1004-AS.
- USB cables should be high quality screened types.
- Ensure that the screens of any external cables are bonded to a good RF earth at the remote end of the cable.

Failure to observe these recommendations may invalidate the EMC compliance.

Quick Start

The following sections explain how to install the ETX-CN700 Single Board Computer onto your host board.

As this single board computer can be installed onto a variety of host boards, the BlueChip Technology MagnumX product has been used as an example host board.

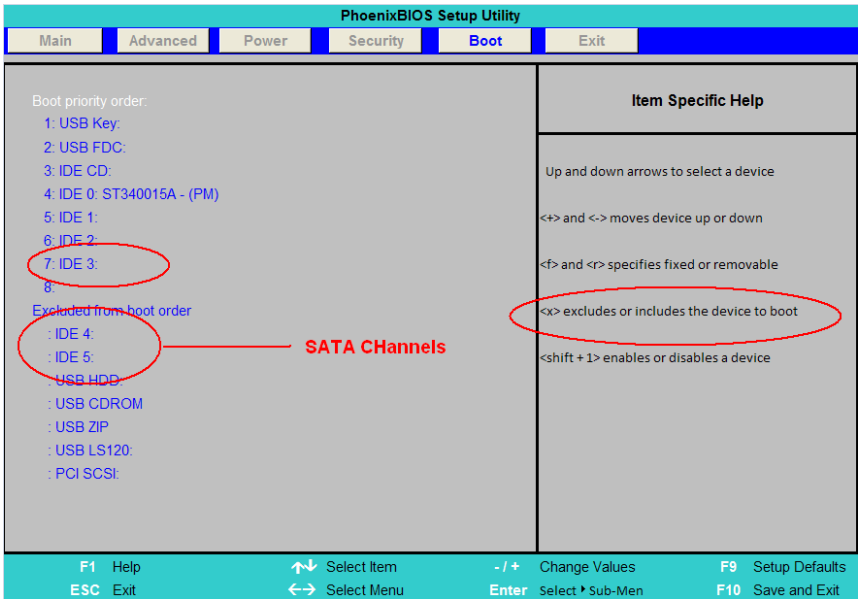
First ensure that you are familiar with the contents of the section "Precautions". It contains important information to avoid damage to the board.

Next, read the appropriate documentation from your System Unit supplier on how to install or upgrade a processor board into the intended system unit.

If choosing your own cooling solution for the CPU, then check the application notes for the particular CPU from the VIA website to ensure that your solution is capable of cooling the processor throughout the desired operating temperature range. Note that the upper operating limit of 60°C is for the board operation in free air, which would equate to the air temperature inside an enclosure with the lid closed. It is important to ensure that the operating temper inside the system unit in the vicinity of the processor board does not exceed the 60°C limit.

Some higher powered CPU options may have a lower operating limit than 60°C, so refer to individual datasheets for precise operating conditions

If using SATA HDD or DVD, then be aware that the SATA ports on the ETX-CN700 are identified in BIOS as “IDE 4” and “IDE 5” and that in order to boot from these devices, they need to be among the 8 devices in the top “Boot Order Priority” field as shown below.



Note that, in order to promote a device from the “Excluded” section, then there must be 7 (or less) devices in the “Boot Order Priority” field. If there are already 8 devices, then some need to be removed first in order to promote others. Using the cursor, select the appropriate device and press “X”. This will Remove/Add the device from the “Boot Order Priority” field as appropriate.

Assembly

Connector locations

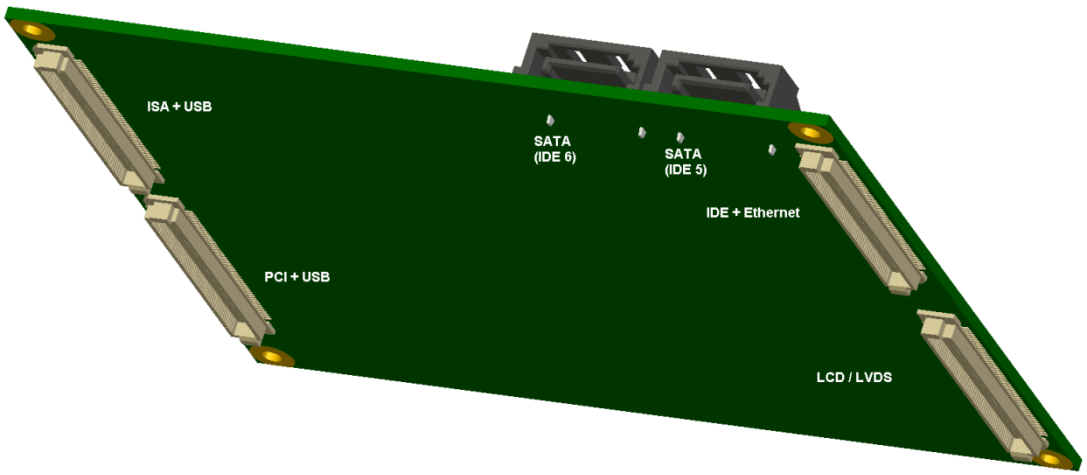


Figure 1: Connector Locations

With an ETX Single Board Computer, the main connections for Keyboard, Mouse, Video, IDE, USB etc are made via the Host Board. On the ETX CN700 there are only two direct connections, both of which are SATA connectors.

Connection to the host board is with four Hirose plug connectors (part number FX8-100P-SV) which mate with corresponding Hirose socket connectors (eg part number FX8-100S-SV). There are four mounting holes of 2.5mm diameter are available for securing the ETX CN700 to the host board

Refer to Appendix 1 for details of the connector pin descriptions

When installing or removing the ETX CN700 module onto the host board, ensure that all power has been removed, including 5V stand- by if present and any external Lithium cell or RTC back-up battery.

Before assembling the ETX CN700 onto the host board, check if any pillars or mounting fittings need to be fitted to the host board.

The Blue Chip Technology MagnumX product has 4 mounting pillars which must first be attached to the host board as shown below in Figure 2.

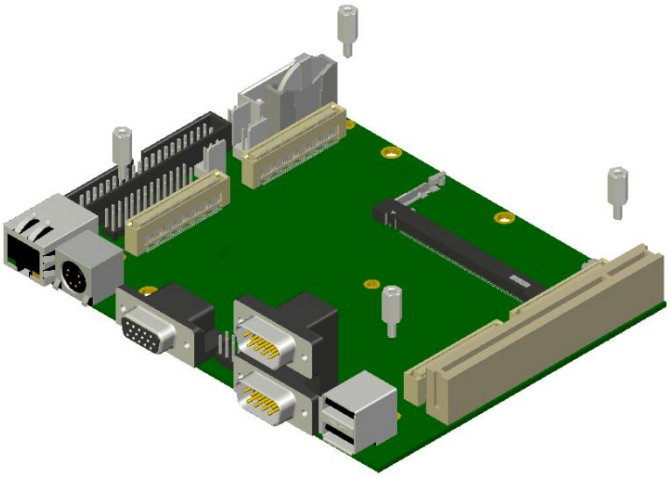


Figure 2: ensure mounting pillars are fitted to host board

The next action is to carefully align the connectors of the ETX CN700 with those on the host board and carefully press together.

Note: The Hirose connectors are offset from each other, so the ETX CN700 will only fit on one orientation. Trying to force the ETX CN700 in the wrong orientation may damage the connectors

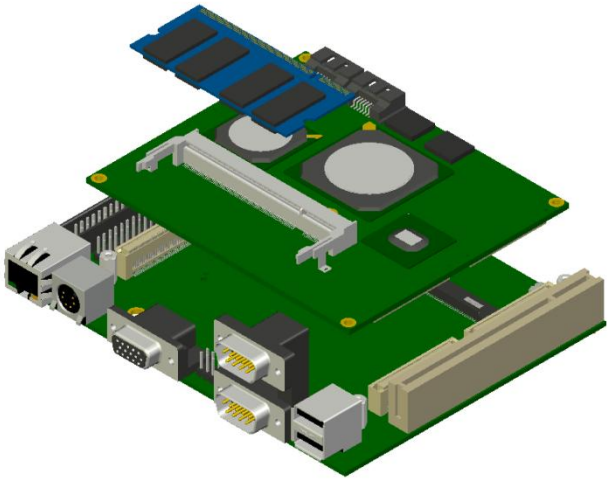


Figure 3: Align ETX CN700 connectors with the host board

If the memory module is not already fitted, then carefully fit the memory module onto the memory socket. The socket is notched to indicate the orientation of the module

At this stage, the cooling solution should be applied. There are several different methods of cooling the ETX CN700

Cooling

Efficient cooling is essential for long and reliable operation of any electronic equipment. The VIA Eden/C7/Nano CPU, the VIA CN700 Northbridge and VIA VT8237 Southbridge do get hot in normal operation, and in an elevated ambient temperature will require additional cooling. Cooling requirements will vary with application, desired operating temperature, CPU load, and memory size and board orientation.

Mounting the PCB vertically will aid natural convection and create a chimney effect. Passive heat sinks can be used for the CPU, Northbridge and Southbridge. A fan, whilst not always desirable, will provide a high degree of cooling even for a relatively slow airflow.

Further options that may be considered are sinking heat to the chassis or enclosure and in extreme situations the use of a heat pipe.

The CPU is equipped with an onboard thermal diode for temperature monitoring. A thermistor is available to monitor the temperature of critical and potential hot spots on the board. Temperatures can be monitored in the BIOS Set-up. If you wish to monitor these temperatures from your application please contact the Blue Chip Technology Technical Support team.

When designing an enclosure, bear in mind that the greater the volume of air that can flow through the enclosure, the greater the cooling effect and the lower the temperature rise above the ambient air temperature. However, the volume produced by any fan will vary with the pressure against which it has to work. The resistance to airflow (the back-pressure on the fan) will depend upon the enclosure, the mounting and restrictions. Therefore, when mounting and cabling the board, it is essential that the free circulation of the cooling airflow is not impeded.

The calculation of airflow through an enclosure is not straightforward, and depends on many factors. The method of meeting the cooling requirements will be specific for each system. Consequently, the system builder is responsible for ensuring adequate cooling. However, interpreting airflow volumes is not intuitive. As an aid to selecting suitable cooling, the following example is offered. A 60 mm axial fan (such as a Papst type 612NGH) blowing over the board can supply up to 46 m^3/hour when unrestricted. Restrictions to the airflow will reduce this volume.

Blue Chip Technology offers several cooling solutions to help manage cooling:

- Heat plate designed to allow contact with a larger cooling area such as direct contact with a metal enclosure
- A passive finned heatsink
- An active solution based on the finned heatsink with a fan (12 m^3/hour) attached

Using the example of MagnumX, the following pictures show how the Active solution can easily be applied

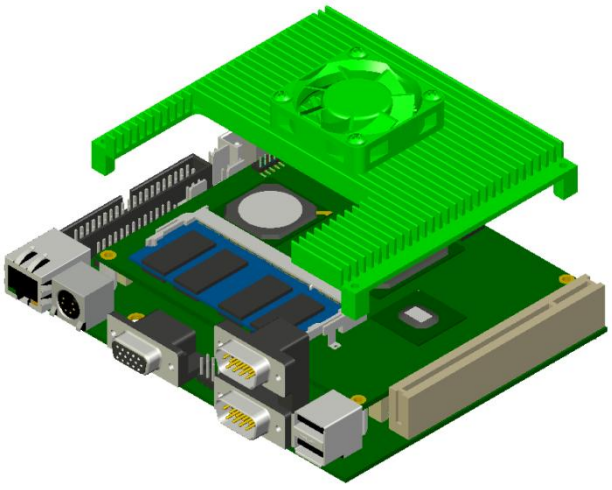


Figure 4: Position Heatsink above ETX CN700 module

The Active solution has thermal pads attached to the bosses on the base of the finned heatsink which make direct contact with the surface of Northbridge, Southbridge and two voltage regulators to help dissipate heat into the heatsink.

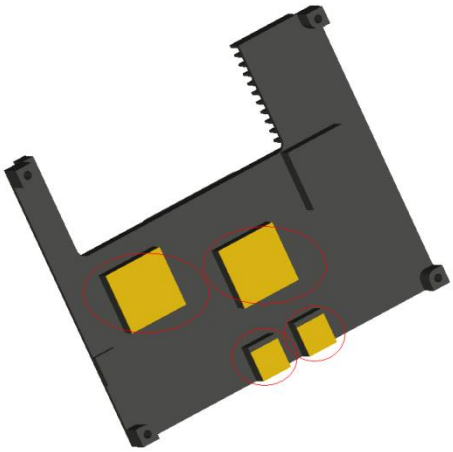


Figure 5: Heatsink bosses and thermal pads

Before fitting the active solution, it is necessary to spread some thermal grease to the surface of the boss which will contact the CPU. Thermal grease is required as thermal pads provide less thermal conductivity than required for the CPU. Note: the minimum amount of thermal grease should be used

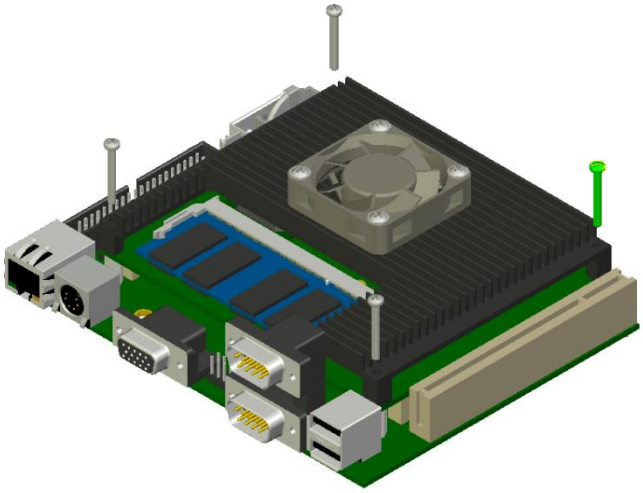


Figure 6: secure the assembly using screws

To finish of the assembly, it is necessary to use screws to secure the active solution in place. This also protects against the ETX coming unseated from the host board during operation

Stack Heights and Clearances

The MagnumX stack heights for the above example are shown below.

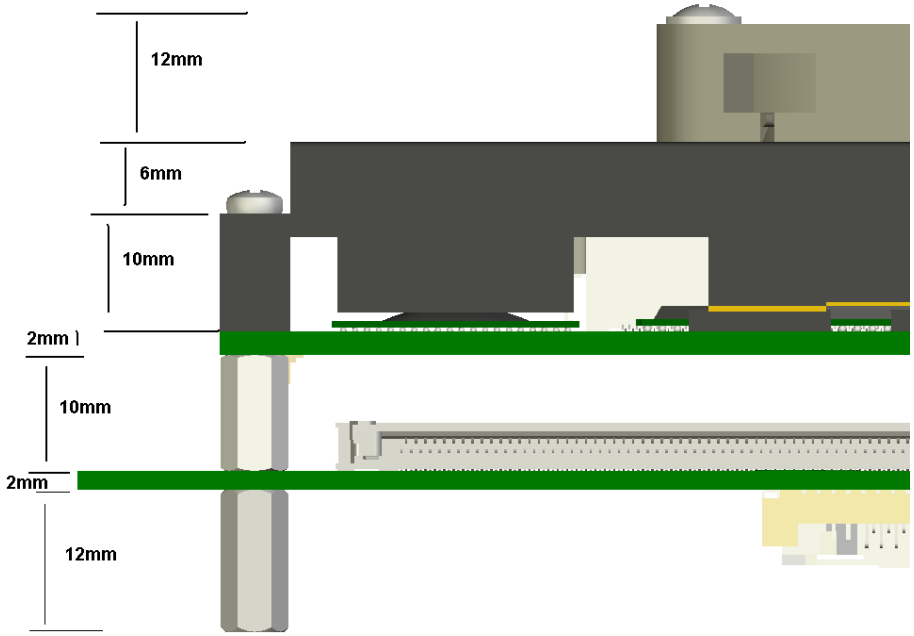


Figure 7: MagnumX with Active Cooling Stack dimensions

Stack heights will depend on the length of the Hirose connectors on the host board. For example, the MagnumX uses longer connectors on the base board to allow for high components on the host board, so there is a board to board gap of 10mm.

On another Blue Chip Technology host board, the BCT-Eval board, there are no components on the host board in the ETX area, so lower height connectors are used. Consequently the board to board gap is only 3mm.

Using the above example, the overall height from the inside base of an enclosure to the top edge of the screw would be 54mm. As the fan draws air down from the top and pushes out through the sides, in this instance, there is a requirement for at least 25mm clear space above the fan to ensure the fan operates efficiently. This could be achieved two ways: firstly, a gap of 25mm between the top of the fan and the inside of the top cover, or secondly, the cover could be just above the fan, with ventilation holes in the cover to allow air to flow freely into the fan as shown in Figure 8 below.

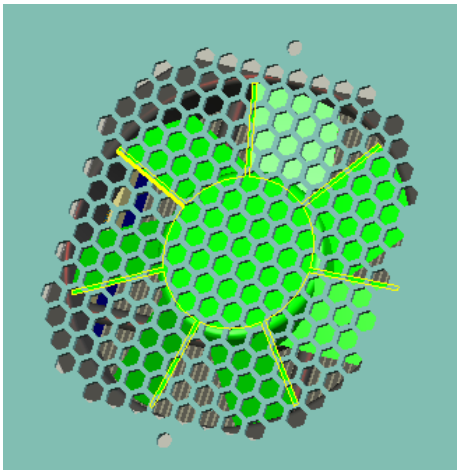


Figure 8: Example of Cover close to top of fan

System Software

Operating System Install

A DVD-ROM is supplied with each board, containing most common operating system drivers. Bear in mind that suppliers continually update their drivers, so it is always a good idea to check on the Internet for later ones.

The following websites are good starting points:
www.viaarena.com
www.viatech.com
www.intel.com

For example for a fresh install of Windows XP operating system, drivers can be installed as follows

First install the CN700 Chipset #1 drivers. This driver includes the graphics driver, and there are several choices as to which particular driver to choose depending on your requirements. Refer to the readme file in the Drivers\SBPC\ETXCN700\Chipset 1 sub directory for more information on the choices

Next install the Chipset 2 driver by executing the setup.exe file in the Drivers\SBPC\ETXCN700\Chipset 2 folder. This installs the necessary IDE/SATA/Raid driver for the VT8237 Southbridge device

For Audio driver, run the setup.exe file from the Drivers\SBPC\ETXCN700\Audio folder.

Lastly, for the LAN driver, use Device Manager and when prompted, point the install to the Drivers\SBPC\ETXCN700\LAN\MS\X86 folder

Operating System API Functions

System Health Monitor

The support for the hardware monitor on the ETX-CN700 processor board will be incorporated into the unified system health monitor API library (SYSMON) and as such supports the following API calls…

DWORD BCTEnableHwMonitor(VOID);
DWORD BCTDisableHwMonitor(VOID);
DWORD BCTReadVoltage(BYTE bVoltageSource, DOUBLE *pdVoltageReading);
DWORD BCTReadTemp(BYTE bTempSource, DOUBLE *pdTempReading);

Watchdog / EEPROM

The support for the watchdog and EEPROM on the ETX-CN700 processor board will be provided through a board specific BCTAPI library and as such support the following API calls…

DWORD BCTOpen(WORD wDevice);
DWORD BCTClose(WORD wDevice);
DWORD BCTWatchdog(BYTE bWdgAction, BYTE bTimeout, BYTE bRange);
DWORD BCTWriteEeprom(WORD wOffset, BYTE bVal);
DWORD BCTReadEeprom(WORD wOffset, PBYTE pbVal);
DWORD BCTEraseEepromByte(WORD wOffset);
DWORD BCTEraseEeprom(VOID);

System BIOS

The ETX-CN700 Single board computer uses the Phoenix BIOS, which has a built-in Setup program that allows users to modify the basic system configuration. This type of information is stored in on-board flash for retention when the power is turned off. Date and time information is in a battery-backed RAM (CMOS RAM) that retains the information each time the power is turned off.

To enter the BIOS setup pages, press the <F2> key just after powering on the unit

If you want to temporarily change the BOOT order, for example to boot from a USB device, then during POST or when the Splash screen is being displayed, press the <ESC> key to enter the BOOT selection Menu.

BIOS Menus

The following pages show the Menu pages found when entering the BIOS. These pages can be used as a reference guide and descriptions of the main user configurable options are provided for information.

The following pages do not go into great depth, so if you require more in-depth data on particular BIOS settings please contact Blue Chip Technology Technical Support staff via the web interface at

http://support.bluechiptechnology.co.uk/

Caution: Changing settings to the wrong values can result in an unreliable or non working unit.

If changing settings, then it is recommended that these are recorded in a safe place for later reference by field engineers

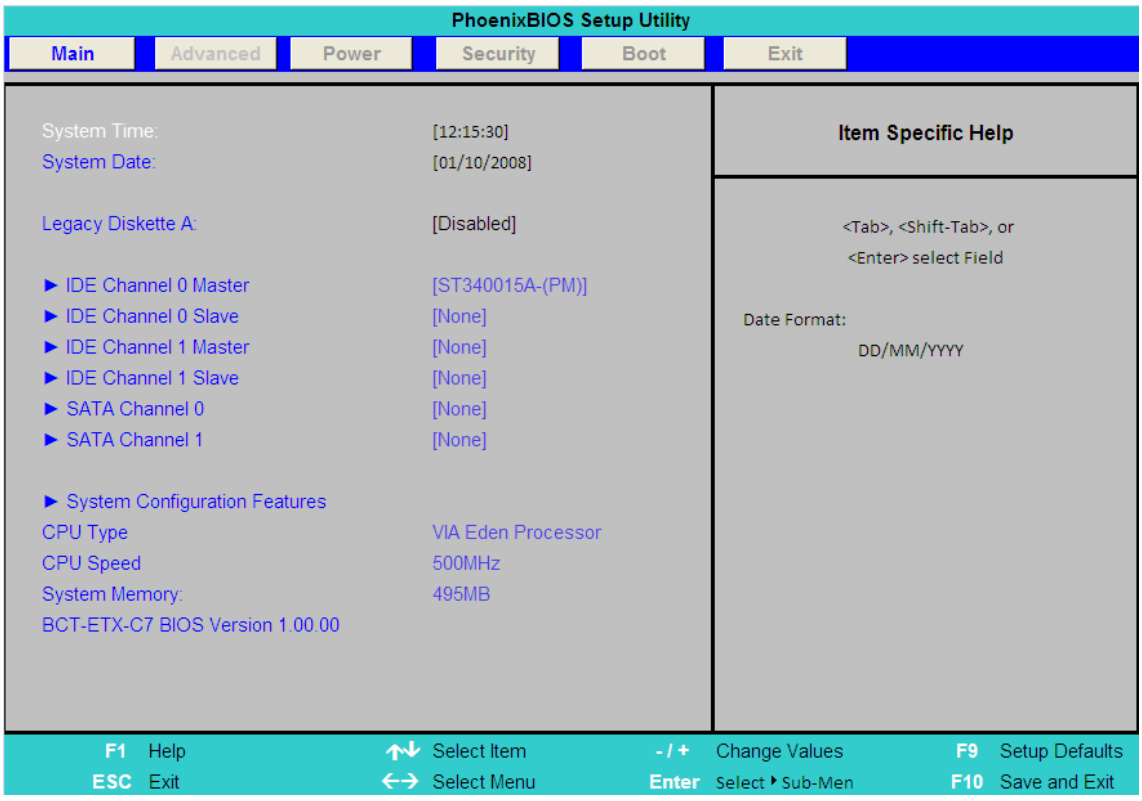
Navigation

Navigation through the various pages is fairly straightforward and hints are given at the bottom of each page.

In general, when on a page, use the Up (↑), Down (↓), Left (←) and right (→) arrows to move around the page, use the Page Up <PgUp> or plus <+> key to increase the numeric value, the Page Down <PgDn> or minus <-> key to decrease the numeric value, and use the Enter <Enter> key to go to the sub menu for that particular option.

When in a Sub Menu, pressing the escape <ESC> key will return to the parent menu

Main Menu

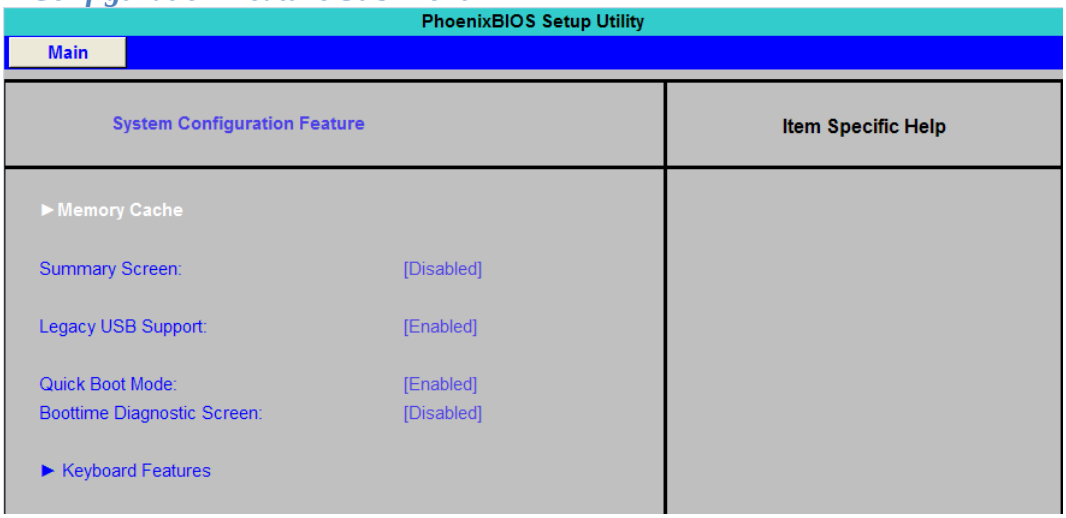


Picture B1

The Main menu allows the setting of Date and Time, as well as providing details of IDE devices fitted to the unit.

Note: In the Boot menu shown later, SATA Channel 0 and 1 are equivalent to IDE 4 and IDE 5 respectively

System Configuration Feature Sub Menu

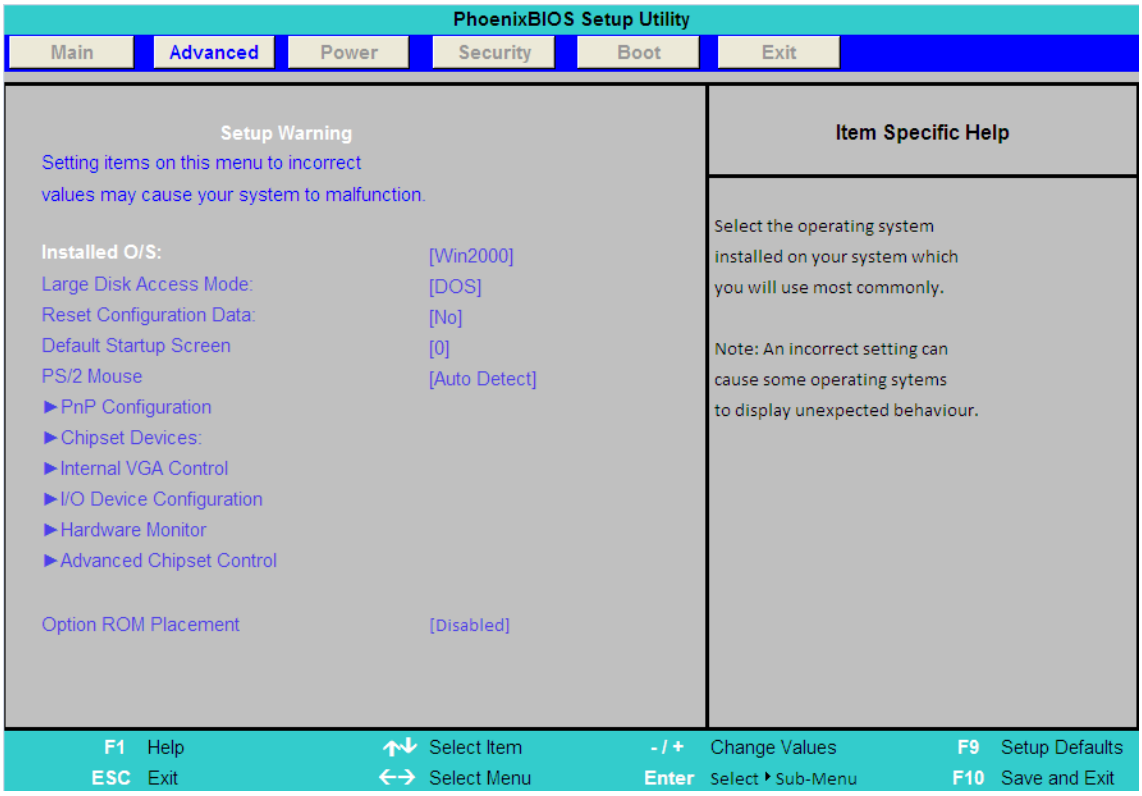


Picture B2

In this sub menu, the important features are

- Legacy USB – Enabled for USB Keyboards, Mice and FDD to be recognised during Boot
- Quick Boot Mode – Enabled for faster boot process
- Boot time Diagnostic Screen – Enabled for a summary of devices and their resources to eb shown after POST and prior to OS load

Advanced Menu



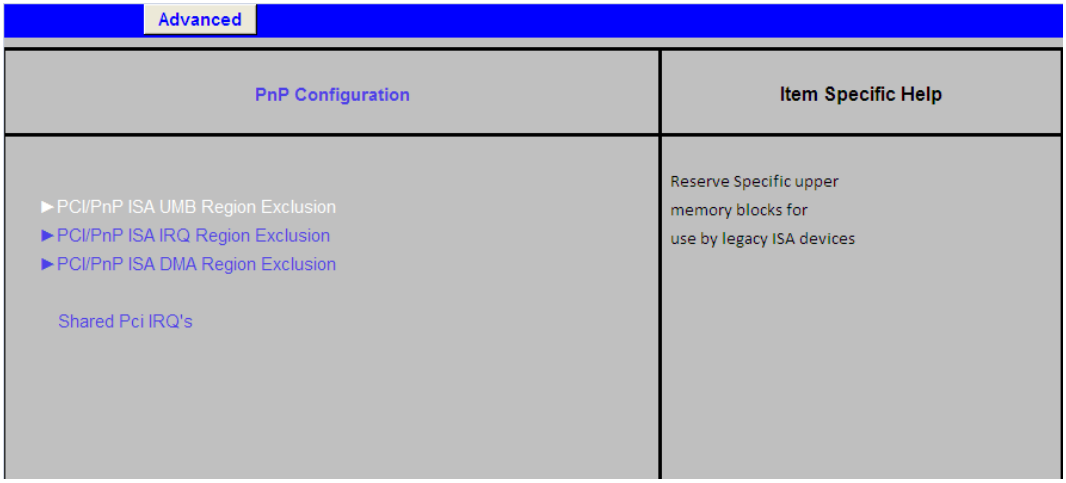
Picture B3

The Advanced Menu pages, provide the means to customise the configuration of the ETX CN700

Reset Configuration Data

If this setting is set to enabled, then when the ETX CN700 is next booted, the BIOS refreshes the configuration data, and frees up resources which were being reserved for hardware no longer installed

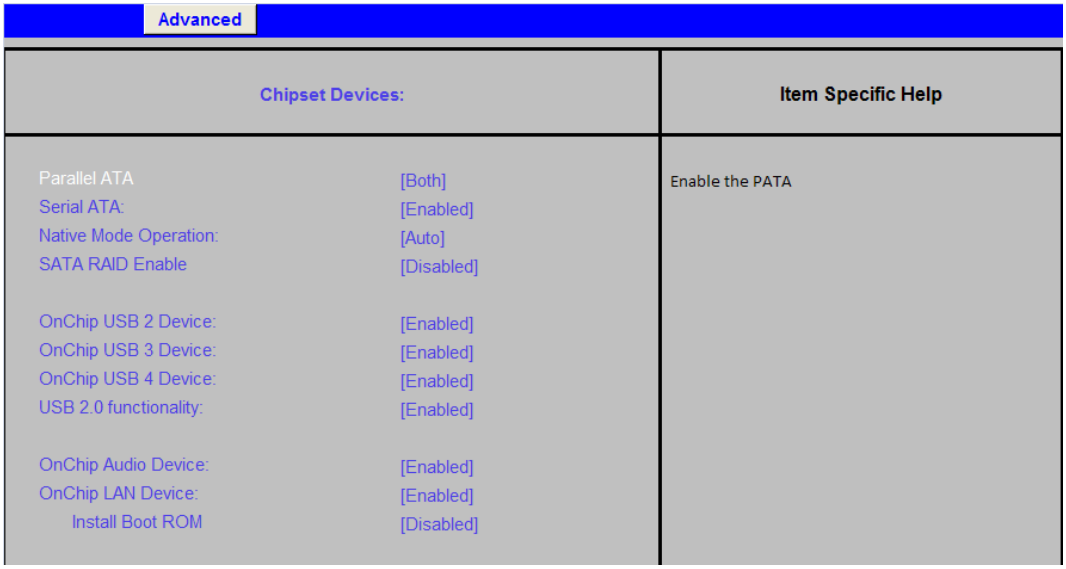
PnP Configuration Sub Menu



Picture B4

This sub menu allows the reservation of system resources for use with legacy ISA devices.

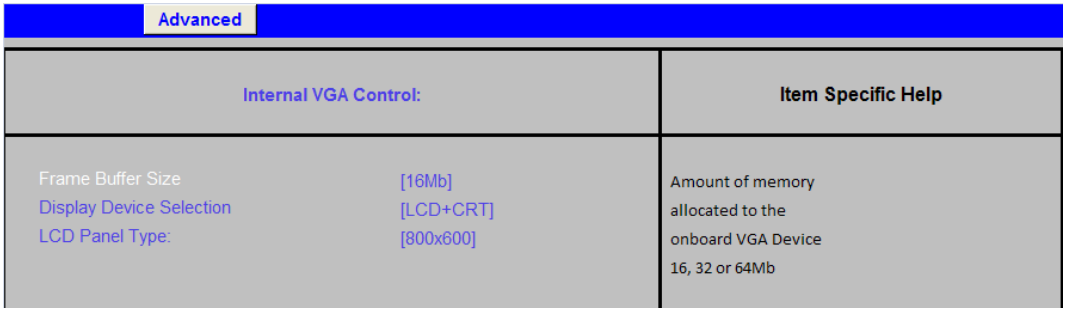
Chipset Devices Sub Menu



Picture B5

The Chipset sub menu allows for PATA, SATA, USB, Audio and LAN functionality to be enabled or disabled

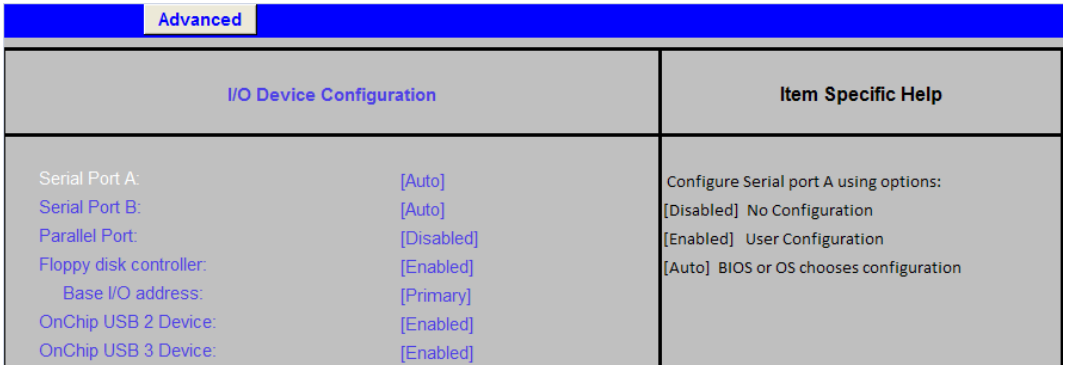
Internal VGA Control Sub Menu



Picture B6

This sub menu allows the size of the frame buffer to be changes as well as selection of display type

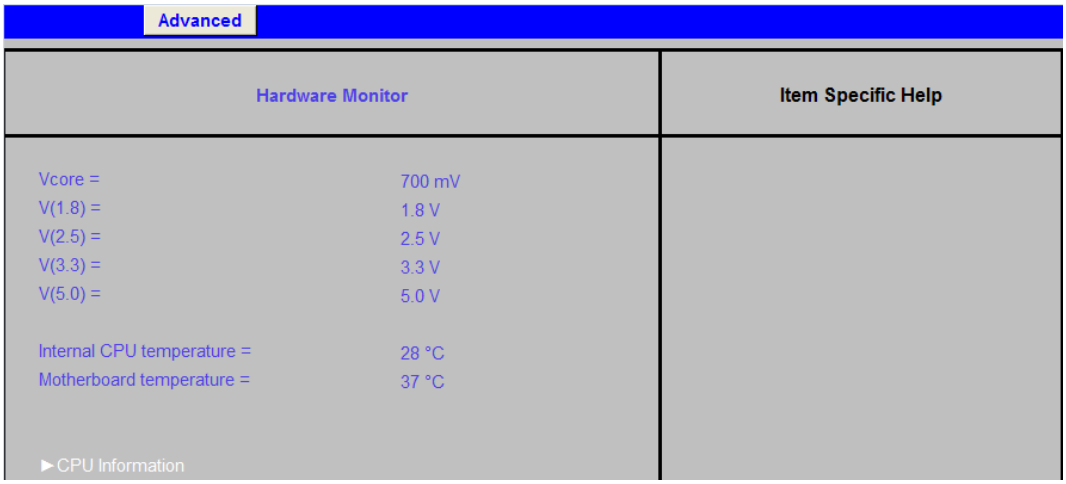
I/O Device Configuration



Picture B7

This sub menu allows for controlling the Serial, Parallel and Floppy interfaces

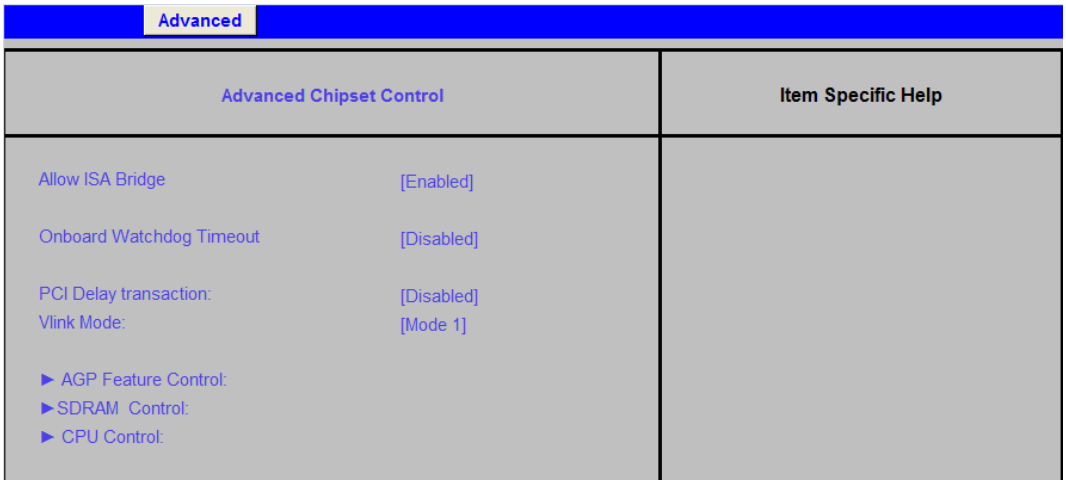
Hardware Monitor



Picture B8

This sub menu shows on board voltages and temperatures for CPU and motherboard. The CPU is an internal Die reading, while the motherboard sensor is on the underside of the PCB

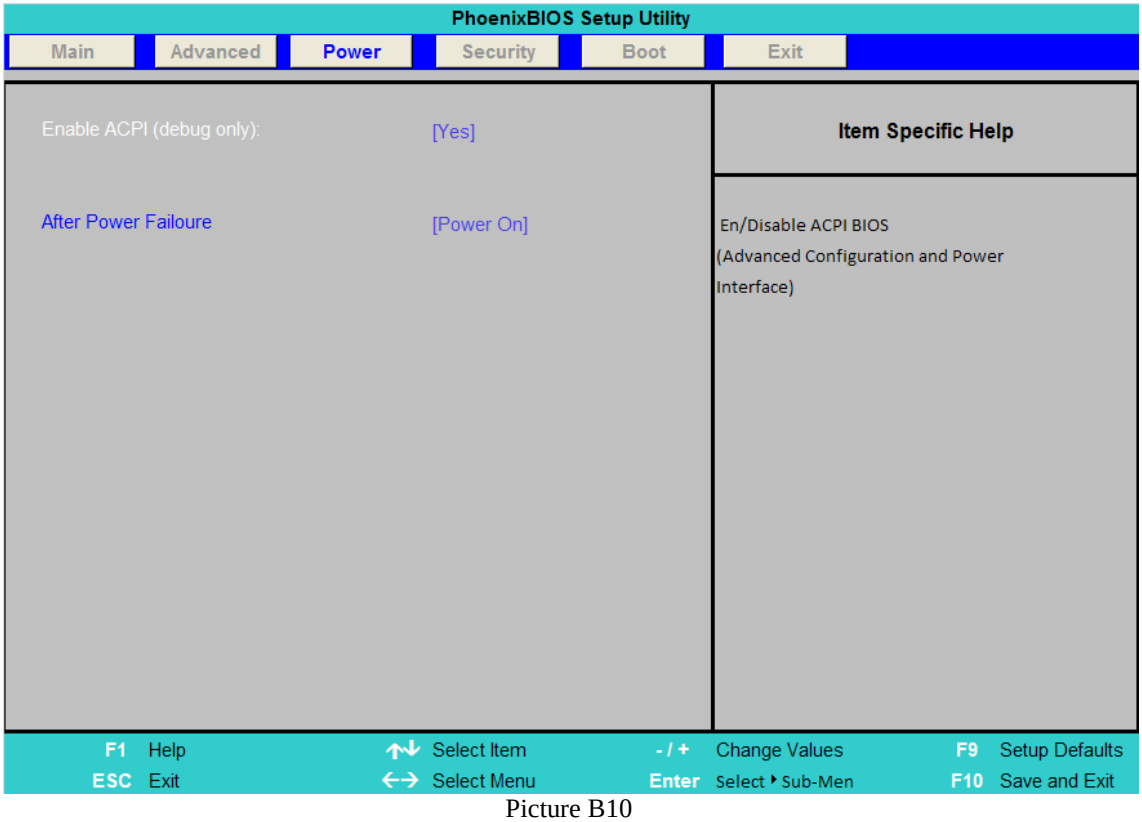
Advanced Chipset Control



Picture B9

Key settings in this submenu are the Allow ISA Bridge, which needs to be enabled if the host board supports ISA cards, and the Onboard Watchdog Timeout.

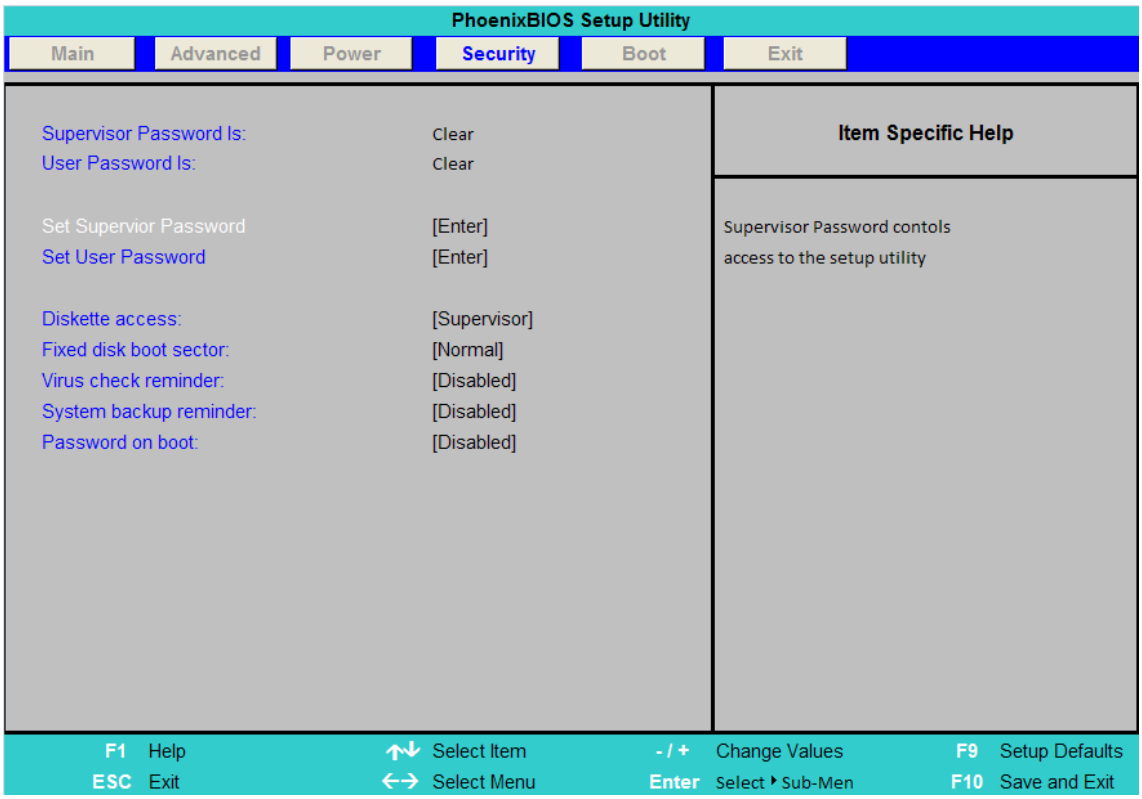
Power Menu



Picture B10

The Power Menu allows the user to set the state for power failure. Options are Off, Last State, and on. When set to on, then as soon as AC power is applied the ETX CN700 will power on

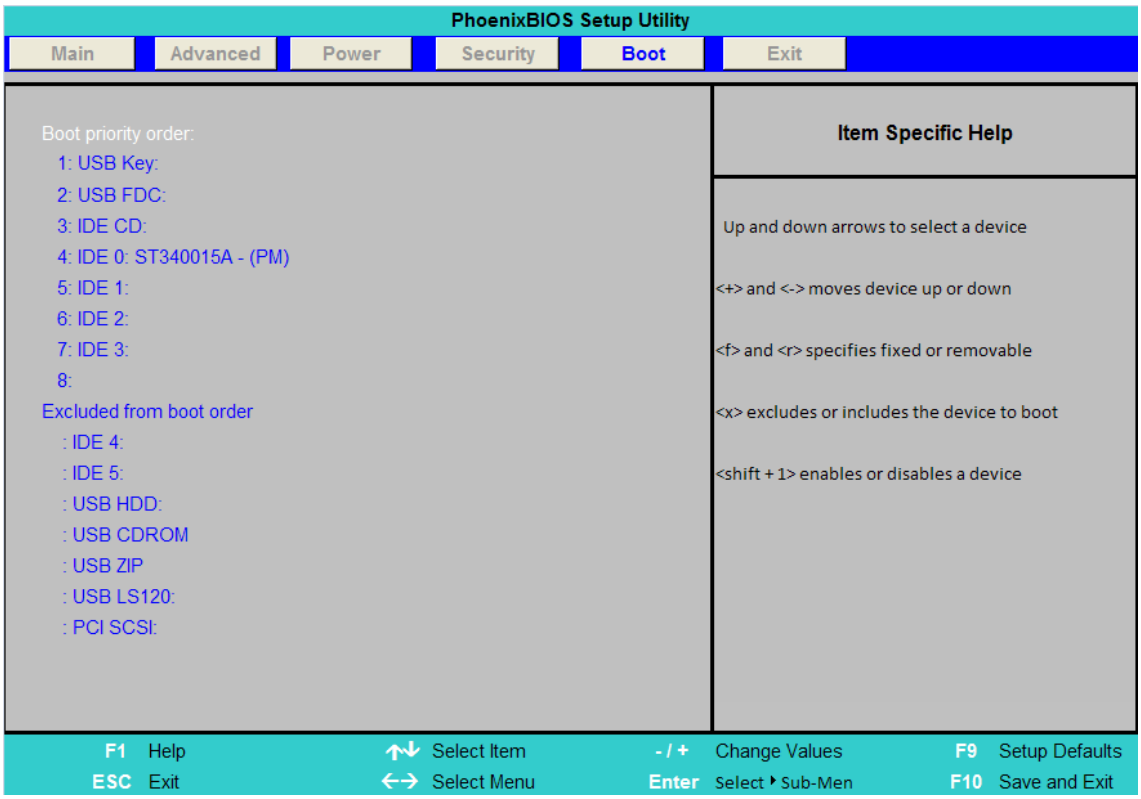
Security Menu



Picture B11

The Security menu allows for BIOS and Boot passwords to be set

Boot Menu



Picture B12

The boot menu allows for a number of boot devices to be set

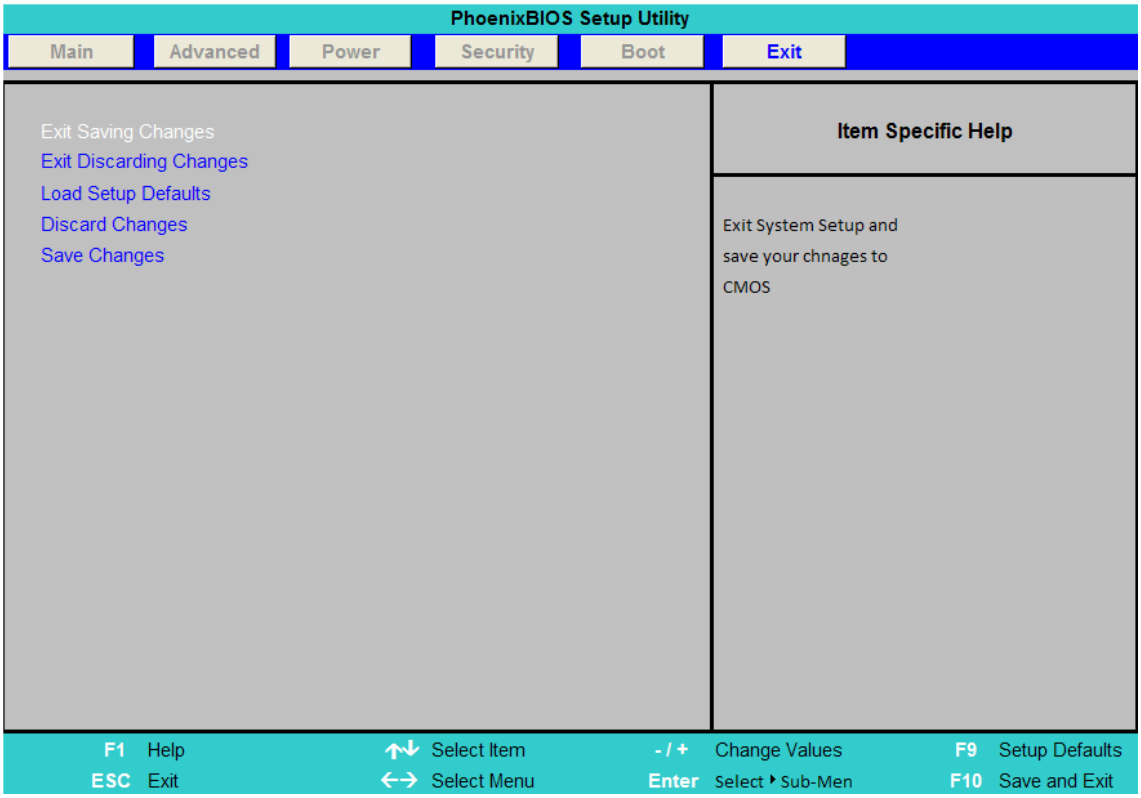
In total 8 boot devices can be selected. If there are 8 devices already listed and another device is required, then one of the 8 needs to be removed from the Boot Order List by first selecting it, and then typing the “X” key

A device form the Excluded list can be added to the Boot Order list by first selecting it, and then typing the “X” key.

Devices in the Boot Order List can be moved up and down the order by selecting them and hitting “+” to increase up the order, or “-“ to move down the order

Note: SATA devices are shown on channels “IDE 4” and “IDE 5”

Exit Menu



Picture B13

As well as offering the means to exit with and without saving settings, this menu also allows for the System BIOS Default Settings to be restored

ETX Connector Details

Connector X1

Pin Number	Signal	Signal Level	Pin Number	Signal	Signal Level
1	GND		2	GND	
3	PCICLK3	3.3 v	4	PCICLK4	3.3 v
5	GND		6	GND	
7	PCICLK1	3.3 v	8	PCICLK2	3.3 v
9	REQ3#	3.3 v	10	GNT3#	3.3 v
11	GNT2#	3.3 v	12	3V	3.3 v
13	REQ2#	3.3 v	14	GNT1#	3.3 v
15	REQ1#	3.3 v	16	3V	3.3 v
17	GNT0#	3.3 v	18	NC	
19	VCC	5 v	20	VCC	5 v
21	SERIRQ	3.3 v	22	REQ0#	3.3 v
23	AD0	3.3 v	24	3V	3.3 v
25	AD1	3.3 v	26	AD2	3.3 v
27	AD4	3.3 v	28	AD3	3.3 v
29	AD6	3.3 v	30	AD5	3.3 v
31	CBE0#	3.3 v	32	AD7	3.3 v
33	AD8	3.3 v	34	AD9	3.3 v
35	GND		36	GND	
37	AD10	3.3 v	38	AUXAL	Audio
39	AD11	3.3 v	40	MIC	Audio
41	AD12	3.3 v	42	AUXAR	Audio
43	AD13	3.3 v	44	ASVCC	5 v Audio
45	AD14	3.3 v	46	SNDL	Audio
47	AD15	3.3 v	48	ASGND	
49	CBE1#	3.3 v	50	SNDR	Audio
51	VCC	5 v	52	VCC	5 v
53	PAR	3.3 v	54	SERR#	3.3 v
55	PERR#	3.3 v	56	NC	
57	PME#	3.3 v	58	USB2#	3.3 v
59	LOCK#	3.3 v	60	DEVSEL#	3.3 v
61	TRDY#	3.3 v	62	USB3#	3.3 v
63	IRDY#	3.3 v	64	STOP#	3.3 v
65	FRAME#	3.3 v	66	USB2	3.3 v
67	GND		68	GND	
69	AD16	3.3 v	70	CBE#2	3.3 v
71	AD17	3.3 v	72	USB3	3.3 v
73	AD19	3.3 v	74	AD18	3.3 v
75	AD20	3.3 v	76	USB0#	3.3 v
77	AD22	3.3 v	78	AD21	3.3 v
79	AD23	3.3 v	80	USB1#	3.3 v
81	AD24	3.3 v	82	CBE3#	3.3 v
83	VCC	5 v	84	VCC	5 v
85	AD25	3.3 v	86	AD26	3.3 v
87	AD28	3.3 v	88	USB0	3.3 v
89	AD27	3.3 v	90	AD29	3.3 v
91	AD30	3.3 v	92	USB1	3.3 v
93	PCIRST#	3.3 v	94	AD31	3.3 v
95	INTC#	3.3 v	96	INTD#	3.3 v
97	INTA#	3.3 v	98	INTB#	3.3 v
99	GND		100	GND	

Connector X2

Pin Number	Signal	Signal Level	Pin Number	Signal	Signal Level
1	GND		2	GND	
3	SD14	5 v	4	SD15	5 v
5	SD13	5 v	6	MASTER#	5 v
7	SD12	5 v	8	DREQ7	5 v
9	SD11	5 v	10	DACK7#	5 v
11	SD10	5 v	12	DREQ6	5 v
13	SD9	5 v	14	DACK6#	5 v
15	SD8	5 v	16	DREQ5	5 v
17	MEMW#	5 v	18	DACK5#	5 v
19	MEMR#	5 v	20	DREQ0	5 v
21	LA17	5 v	22	DACK0#	5 v
23	LA18	5 v	24	IRQ14	5 v
25	LA19	5 v	26	IRQ15	5 v
27	LA20	5 v	28	IRQ12	5 v
29	LA21	5 v	30	IRQ11	5 v
31	LA22	5 v	32	IRQ10	5 v
33	LA23	5 v	34	IOCS16#	5 v
35	GND		36	GND	
37	SBHE#	5 v	38	MEMCS16#	5 v
39	SA0	5 v	40	OSC	5 v
41	SA1	5 v	42	BALE	5 v
43	SA2	5 v	44	TC	5 v
45	SA3	5 v	46	DACK2#	5 v
47	SA4	5 v	48	IRQ3	5 v
49	SA5	5 v	50	IRQ4	5 v
51	VCC	5 v	52	VCC	5 v
53	SA6	5 v	54	IRQ5	5 v
55	SA7	5 v	56	IRQ6	5 v
57	SA8	5 v	58	IRQ7	5 v
59	SA9	5 v	60	SYSCLK	5 v
61	SA10	5 v	62	REFRESH#	5 v
63	SA11	5 v	64	DREQ1	5 v
65	SA12	5 v	66	DACK1#	5 v
67	GND		68	GND	
69	SA13	5 v	70	DREQ3	5 v
71	SA14	5 v	72	DACK3#	5 v
73	SA15	5 v	74	IOR#	5 v
75	SA16	5 v	76	IOW#	5 v
77	SA18	5 v	78	SA17	5 v
79	SA19	5 v	80	SMEMR#	5 v
81	IOCHRDY	5 v	82	AEN	5 v
83	VCC	5 v	84	VCC	5 v
85	SD0	5 v	86	SMEMW#	5 v
87	SD2	5 v	88	SD1	5 v
89	SD3	5 v	90	0WS#	5 v
91	DREQ2	5 v	92	SD4	5 v
93	SD5	5 v	94	IRQ9	5 v
95	SD6	5 v	96	SD7	5 v
97	IOCHCK#	5 v	98	RSTDRV	5 v
99	GND		100	GND	

Connector X3

Pin Number	Signal	Signal Level	Pin Number	Signal	Signal Level
1	GND		2	GND	
3	RED	Video	4	BLUE	Video
5	HSYNC	3.3 v	6	GREEN	Video
7	VSYNC	3.3 v	8	DDCK	3.3 v
9	DETECT#		10	DDDA	3.3 v
11	2ND LVDSCLK#/***B4***	2.5 v / 3.3 v	12	2nd LVDS3#/ *SHFCLK*	2.5 v / 3.3 v
13	2ND LVDSCLK/***B5***	2.5 v / 3.3 v	14	***2nd LVDS3/EN***	2.5 v / 3.3 v
15	GND		16	GND	
17	2ND LVDS 1/***B1***	2.5 v / 3.3 v	18	2ND LVDS2/***B3***	2.5 v / 3.3 v
19	2ND LVDS1#/***B0***	2.5 v / 3.3 v	20	2ND LVDS2#/***B2***	2.5 v / 3.3 v
21	GND		22	GND	
23	1st LVDS3#/***G2***	2.5 v / 3.3 v	24	2ND LVDS0/***G5***	2.5 v / 3.3 v
25	1st LVDS3/***G3***	2.5 v / 3.3 v	26	2ND LVDS0#/***G4***	2.5 v / 3.3 v
27	GND		28	GND	
29	1ST LVDS2#/***R4***	2.5 v / 3.3 v	30	1ST LVDSCLK/***G1***	2.5 v / 3.3 v
31	1ST LVDS2/***R5***	2.5 v / 3.3 v	32	1ST LVDSCLK#/***G0***	2.5 v / 3.3 v
33	GND		34	GND	
35	1ST LVDS0/***R1***	2.5 v / 3.3 v	36	1ST LVDS1/***R3***	2.5 v / 3.3 v
37	1ST LVDS0#/***R0***	2.5 v / 3.3 v	38	1ST LVDS1#/***R2***	2.5 v / 3.3 v
39	VCC	5 v	40	VCC	5 v
41	I2CDAT	3.3 v	42	LTGIO/***FLM***	2.5 v / 3.3 v
43	I2CCLK	3.3 v	44	BLON#	3.3 v
45	BIASON/***LP***	2.5 v / 3.3 v	46	DIGON	3.3 v
47	NC		48	NC	
49	NC		50	NC	
51	LPT/***FLPY#***	3.3 v	52	NC	
53	VCC		54	GND	
55	STB#/***RSVD***	3.3 v	56	AFD#/***DENSEL***	3.3 v
57	RSVD	3.3 v	58	PD7/***RSVD***	3.3 v
59	IRRX	3.3 v	60	ERR#/***HDSEL#***	3.3 v
61	IRTX	3.3 v	62	PD6/***RSVD***	3.3 v
63	RXD2	3.3 v	64	INIT#/***DIR#***	3.3 v
65	GND		66	GND	
67	RTS2#	3.3 v	68	PD5/***RSVD***	3.3 v
69	DTR2#	3.3 v	70	SLIN#/***STEP#***	3.3 v
71	DCD2#	3.3 v	72	PD4/***DSKCHG#***	3.3 v
73	DSR2#	3.3 v	74	PD3/***RDATA#***	3.3 v
75	CTS2#	3.3 v	76	PD2/***WP#***	3.3 v
77	TXD2	3.3 v	78	PD1/***TRK0#***	3.3 v
79	RI2#	3.3 v	80	PD0/***INDEX***#	3.3 v
81	VCC	5 v	82	VCC	5 v
83	RXD1	3.3 v	84	ACK#/***DRV***	3.3 v
85	RTS1#	3.3 v	86	BUSY#/***MOT***	3.3 v
87	DTR1#	3.3 v	88	PE/***WDATA#***	3.3 v
89	DCD1#	3.3 v	90	SLCT#/***WGATE#***	3.3 v
91	DSR1#	3.3 v	92	MSCLK	3.3 v
93	CTS1#	3.3 v	94	MSDAT	3.3 v
95	TXD1	3.3 v	96	KBCLK	3.3 v
97	RI1#	3.3 v	98	KBDAT	3.3 v
99	GND		100	GND	

NOTE: These signals are the definition for the LCD build version of the ETX CN700

NOTE: These signals are the definition when signal LPT/FLPY# (Pin51 of X3) is pulled low at power on.

Connector X4

Pin Number	Signal	Signal Level	Pin Number	Signal	Signal Level
1	GND		2	GND	
3	5VSB	5 v	4	PWRGDIN	3.3 v or 5 v
5	PSON	5 v	6	SPEAKER	5 v
7	PWRBTN#	3.3 v	8	BATT	Battery
9	KBINH	3. 3 v / 5 v	10	ACTLED/LILED	3.3 v
11	RSMRST#	OD	12	LILED/3V3VSUS	3.3 v
13	RSVD		14	SPEEDLED	3.3 v
15	RSVD		16	I2CLK	3.3 v
17	VCC	5 v	18	VCC	5 v
19	OVCR#	5 v	20	RSVD	
21	EXTSMI#	3.3 v	22	I2DAT	3.3 v
23	SMBCLK	3.3 v	24	SMBDATA	3.3 v
25	SIDE_CS3#	3.3 v	26	SMBALERT#	3.3 v
27	SIDE_CS1#	3.3 v	28	DASP_S	3.3 v
29	SIDE_A2	3.3 v	30	PIDE_CS3#	3.3 v
31	SIDE_A0	3.3 v	32	PIDE_CS1#	3.3 v
33	GND		34	GND	
35	PDIAG_S	3.3 v	36	PIDE_A2	3.3 v
37	SIDE_A1	3.3 v	38	PIDE_A0	3.3 v
39	SIDE_IRQ	3.3 v	40	PIDE_A1	3.3 v
41	BATLOW#	3.3 v	42	SIDE_33/66#	3.3 v
43	SIDE_AK#	3.3 v	44	PIDE_IRQ	3.3 v
45	SIDE_RDY	3.3 v	46	PIDE_AK#	3.3 v
47	SIDE_IOR#	3.3 v	48	PIDE_RDY	3.3 v
49	VCC		50	VCC	
51	SIDE_IOW#	3.3 v	52	PIDE_IOR#	3.3 v
53	SIDE_DRQ	3.3 v	54	PIDE_IOW#	3.3 v
55	SIDE_D15	3.3 v	56	PIDE_DRQ	3.3 v
57	SIDE_D0	3.3 v	58	PIDE_D15	3.3 v
59	SIDE_D14	3.3 v	60	PIDE_D0	3.3 v
61	SIDE_D1	3.3 v	62	PIDE_D14	3.3 v
63	SIDE_D13	3.3 v	64	PIDE_D1	3.3 v
65	GND		66	GND	
67	SIDE_D2	3.3 v	68	PIDE_D13	3.3 v
69	SIDE_D12	3.3 v	70	PIDE_D2	3.3 v
71	SIDE_D3	3.3 v	72	PIDE_D12	3.3 v
73	SIDE_D11	3.3 v	74	PIDE_D3	3.3 v
75	SIDE_D4	3.3 v	76	PIDE_D11	3.3 v
77	SIDE_D10	3.3 v	78	PIDE_D4	3.3 v
79	SIDE_D5	3.3 v	80	PIDE_D10	3.3 v
81	VCC	5 v	82	VCC	5 v
83	SIDE_D9	3.3 v	84	PIDE_D5	3.3 v
85	SIDE_D6	3.3 v	86	PIDE_D9	3.3 v
87	SIDE_D8	3.3 v	88	PIDE_D6	3.3 v
89	RING#	3.3 v	90	PIDE_33/66#	3.3 v
91	RXD#	3.3 v	92	PIDE_D8	3.3 v
93	RXD	3.3 v	94	SIDE_D7	3.3 v
95	TXD#	3.3 v	96	PIDE_D7	3.3 v
97	TXD	3.3 v	98	HDRST#	3.3 v
99	GND		100	GND	

Signal Descriptions
Connector X1 (PCI-Bus, USB, Sound)

GND
Ground. All the GND pins on the ETX CN700 module should be connected to the baseboard ground plane.
VCC
+5V ±5% power supply. All VCC pins on the ETX CN700 module should be connected to the baseboard +5V plane.
3V
+3.3V ±5% supply voltage generated onboard the ETX module. These three pins may be used as a power supply for external devices. The maximum permissible current drawn collectively from these pins is 500mA.
NOTE: Do not connect 3.3V pins to an external 3.3V supply.
RSVD
These pins are reserved for future use or for manufacturing and test purposes. Do not connect external signals to these pins.

All signals are 3.3V level PCI signals referenced to and tolerant of 5V signals. All the required PCI signal pull-ups are integrated on the ETX CN700 board and are connected to either a 3.3V or 5V supply, as detailed in the PCI specification. Any external PCI devices that have "5V tolerance" pins should have these pins connected to an appropriate 5V reference voltage as per the manufacturer's recommendation.
PCICLK1..4
PCI clock outputs for up to 4 external PCI slots or devices.
The baseboard designer should route these clocks for 1300pS total delay from the ETX CN700 connector pin to the clock pin of the PCI device.
REQ[0..3]#
Bus Request signals for up to 4 external bus mastering PCI devices. When asserted, a PCI device is requesting PCI bus ownership from the arbiter.
GNT[0..3]#
Grant signals to PCI Masters. When asserted by the arbiter, the requesting PCI master has been granted ownership of the PCI bus.
AD[0..31]
PCI Address and Data Bus Lines. These multiplexed lines carry the address and data information for PCI transactions. A Bus transaction consists of an Address phase followed by one or more Data phases.
CBE[0..3]#
PCI Bus Command and Byte Enables. Bus command and byte enables are multiplexed in these lines for address and data phases, respectively.
PAR
Parity bit for the PCI bus. Generated as even parity across AD[31:0] and CBE[3:0]#.
SERR#
System Error. This signal reports address parity errors, data errors on special cycles or any other system error where the result will be catastrophic.
GPERR#
Parity Error. This signal reports data parity errors on all bus transaction except special cycles.
PME#
Power management event.
LOCK#
Lock Resource Signal. This pin indicates that either the PCI master or the bridge intends to run exclusive transfers.
DEVSEL#
Device Select. When the target device has decoded the address as its own cycle, it will assert DEVSEL#.
TRDY#
Target Ready. This pin indicates that the target is ready to complete the current data phase of a transaction.
IRDY#
Initiator Ready. This signal indicates that the initiator is ready to complete the current data phase of a transaction.
STOP#
Stop. This signal indicates that the target is requesting that the master to stop the current transaction.

FRAME#
Cycle Frame of PCI Buses. This indicates the beginning and duration of a PCI access. The access will be either an output driven by the Northbridge on behalf of the CPU, or an input during PCI master access.
PCIRST#
PCI Bus Reset. This is an output signal to reset the entire PCI Bus. This signal is asserted during system reset.
INTA#, INTB#, INTC#, INTD#
PCI interrupts. These interrupts are sharable and are typically wired in rotation to PCI slots or devices.
IDSEL
This pin is not present on the ETX module connector, but it is present on each PCI slot connector or device. IDSEL is an input to the device that is used to set the device's configuration address for PCI configuration cycles. The IDSEL pin of each device is typically connected to one of the AD lines in order to set a unique configuration address. In ETX systems, the four external bus slots or devices are assumed to use AD[19..22] for IDSEL connections.

USB Signals
USB signal termination components are integrated on the ETX board. In applications using external USB devices, baseboard designers will typically include USB protection components on the baseboard, including power supply current limiting or fusing components. USB data signals should be routed as differential pairs.

USB0, USB0#
Universal Serial Bus Port 0. These are the serial differential data pairs for USB Port 0. USB0 – positive signal. USB0# – negative signal.
USB1, USB1#
Universal Serial Bus Port 1. These are the serial differential data pairs for USB Port 1. USB1 – positive signal. USB1# – negative signal.
USB2, USB2#
Universal Serial Bus Port 2. These are the serial differential data pairs for USB Port 2. USB2 – positive signal. USB2# – negative signal.
USB3, USB3#
Universal Serial Bus Port 3. These are the serial differential data pairs for USB Port 3. USB3 – positive signal. USB3# – negative signal.

Audio Signals
SNDL/ SNDR
Line-level stereo output left/ right. These outputs have a nominal level of 1 volt RMS into a 10K impedance load. These outputs cannot drive low-impedance speakers directly.
AUXAL/ AUXAR
Auxiliary A input left/ right. Normally intended for connection to an internal or external CDROM analog output or a similar line-level audio source. Minimum input impedance is 5KOhm.
Nominal input level is 1 volt RMS.
MIC
Microphone input. Minimum input impedance is 5KOhm, max. input voltage is 0.15 Vpk-pk.
ASGND
Analog ground for sound controller. Use this signal ground for an external amplifier in order to achieve lowest audio noise levels.
ASVCC
Analog supply voltage for sound controller. This is an output which is used for production test only. Do not make external connections to this pin.

Miscellaneous
SERIRQ
Serial interrupt request. This pin is used to support the serial interrupt protocol.

Connector X2

ISA Signals

All required signal pull-ups are integrated into the ETX CN700 module. In some applications it may be desirable to add additional signal termination components to the baseboard.

SD[0..15]

These signals provide data bus bits 0 to 15 for any peripheral devices. All 8-bit devices use SD0[0..7] for data transfers. 16-bit devices use SD[0..15]. To support 8-bit devices, the data on SD[8..15] is gated to SD[0..7] during 8-bit transfers to these devices. 16-bit CPU cycles will be automatically converted into two 8-bit cycles for 8-bit peripherals.

SA[0..19]

Address bits 0 through 15 are used to address I/O devices. Address bits 0 through 19 are used to address memory within the system. These 20 address lines, in addition to LA[17..23] allow access of up to 16MB of memory. SA[0..19] are gated on the ISA-bus when BALE is high and latched on to the falling edge of BALE.

SBHE#

Bus High Enable indicates a data transfer on the upper byte of the data bus SD[8..15]. 16-bit I/O devices use SBHE# to enable data bus buffers on SD[8..15].

BALE

BALE is an active-high pulse generated at the beginning of any bus cycle initiated by a CPU module. It indicates when the SA[0..19], LA17.23, AEN, and SBHE# signals are valid.

AEN

AEN is an active-high output that indicates a DMA transfer cycle. Only resources with a active DACK# signal should respond to the command lines when AEN is high.

MEMR#

MEMR# instructs memory devices to drive data onto the data bus. MEMR# is active for all memory read cycles.

SMEMR#

SMEMR# instructs memory devices to drive data onto the data bus. SMEMR# is active for memory read cycles to addresses below 1MB.

MEMW#

MEMW# instructs memory devices to store the data present on the data bus. MEMW# is active for all memory write cycles.

SMEMW#

SMEMW# instructs memory devices to store the data present on the data bus. SMEMW# is active for all memory write cycles to address below 1MB.

IOR#

I/O read instructs an I/O device to drive its data onto the data bus. It may be driven by the CPU or by the DMA controller. IOR# is inactive (high) during refresh cycles.

IOW#

I/O write instructs an I/O device to store the data present on the data bus. It may be driven by the CPU or by the DMA controller. IOW# is inactive (high) during refresh cycles.

IOCHK#

IOCHK# is an active-low input signal that indicates that an error has occurred on the module bus. If I/O checking is enabled on the CPU module, an IOCHK# assertion by a peripheral device sends a NMI to the processor.

IOCHRDY

The I/O Channel Ready is pulled low in order to extend the read or write cycles of any bus access when required. The CPU, DMA controllers or refresh controller can initiate the cycle. Any peripheral that cannot present read data or strobe in write data within this amount of time use IOCHRDY to extend these cycles. This signal should not be held low for more than 2.5 µs for normal operation. Any extension to more than 2.5 µs does not guarantee proper DRAM memory content due to the fact that memory refresh is disabled while IOCHRDY is low.

MEMCS16#

The MEMCS16# signal determines when a 16-bit to 8-bit conversion is needed for memory bus cycles. A conversion is done any time the CPU module requests a 16-bit memory cycle while the MEMCS16# line is high. If MEMCS16# is high, 16-bit CPU cycles are automatically converted on the bus into two 8-bit cycles. If MEMCS16# is low, an access to peripherals is performed 16 bits wide.

IOCS16#
The IOCS16# signal determines when a 16-bit to 8-bit conversion is needed for I/O bus cycles. A conversion is done any time the CPU module requests a 16-bit I/O cycle while the IOCS16# line is high. If IOCS16# is high, 16-bit CPU cycles are automatically converted on the bus into two 8-bit cycles. If IOCS16# is low, an access to peripherals is performed 16 bits wide.
REFRESH#
REFRESH# is pulled low whenever a refresh cycle is initiated. A refresh cycle is activated every 15.6 us in order to prevent loss of DRAM data.
0WS#
The Zero wait state signal tells the CPU to complete the current bus cycle without inserting the default wait states. By default the CPU inserts 4 wait states for 8-bit transfers and 1 wait state for 16-bit transfers.
MASTER#
This signal is used with a DRQ line to gain control of the system bus. A processor or a DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a DACK#. Upon receiving the DACK#, a bus master may pull MASTER# low, which will allow it to control the system address, data and control lines. After MASTER# is low, the bus master must wait one system clock period before driving the address and data lines, and two clock periods before issuing a read or write command. If this signal is held low for more than 15 us, system memory may be lost as memory refresh is disabled during this process.
SYSCLK
SYSCLK is supplied by the CPU module and has a nominal frequency of about 8 MHz with a duty cycle of 40-60 percent. The frequency supplied by different CPU modules may vary. This signal is supplied at all times except when the CPU module is in sleep mode.
OSC
OSC is supplied by the CPU module. It has a nominal frequency of 14.31818 MHz and a duty cycle of 40-60 percent. This signal is supplied at all times except when the CPU module is in sleep mode.
RESETDRV
This active-high output is system reset generated from CPU modules. It is responsible for resetting external devices on the ISA Bus.
DREQ[0, 1, 2, 3, 5, 6, 7]
The asynchronous DMA request inputs are used by external devices to indicate when they need service from the CPU modules DAM controllers. DREQ0..3 are used for transfers between 8-bit I/O adapters and system memory. DREQ5..7 are used for transfers between 16-bit I/O adapters and system memory. DRQ4 is not available externally. All DRQ pins have pull-up resistors on the CPU modules.
DACK[0, 1, 2, 3, 5, 6, 7]#
DMA acknowledge 0..3 and 5.7 are used to acknowledge DMA requests. They are active-low.
TC
The active-high output Terminal Count indicates that one of the DMA channels has transferred all data.
IRQ[3..7, 9,15]
These are the asynchronous interrupt request lines. IRQ0, 1, 2 and 8 are not available as external interrupts because they are used internally on the CPU module. All IRQ signals are active-high. The interrupt requests are prioritized. IRQ9 through IRQ12 and IRQ14 through IRQ15 have the highest priority (IRQ9 is the highest). IRQ3 through IRQ7 have the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the CPU acknowledges the interrupt request (interrupt service routine).

Connector X3
VGA Signals

HSYNC
Horizontal Sync: This output supplies the horizontal synchronization pulse to the CRT monitor.
VSYNC
Vertical Sync: This output supplies the vertical synchronization pulse to the CRT monitor.
Red, Green, Blue
Red, green and blue analog video output signals for CRT monitors. These lines should be terminated with 75 ohms to ground at the video connector.
DDCK, DDDA
These two pins can be used for a DDC interface between the graphics controller chip and the CRT monitor.

LVDS Flat Panel Interface Signals
NOTE: The ETX CN700.module is available with either LVDS or 18 bit direct drive LCD STN/TFT interface. This option must be specified at the time of purchase. The ETX CN700 does not support 24 bit panels in either LVDS or direct drive LCD options

1st LVDS0, 1st LVDS0#
1st LVDS Channel, link0 differential pairs LCD data output. These signals are differential and should be routed as differential pairs. 1st LVDS0# is the complement of 1st LVDS0.
1st LVDS1, 1st LVDS1#
As above, link1.
1st LVDS2, 1st LVDS2#
As above, link2.
1st LVDS3, 1st LVDS3#
As above, link2.
1st LVDSCLK, 1st LVDSCLK#
As above, clock link.
2nd LVDS0, 2nd LVDS0#
2nd LVDS Channel, link0 differential pairs LCD data output. These signals are differential and should be routed as differential pairs. 2nd LVDS0# is the complement of 2nd LVDS0.
2nd LVDS1, 2nd LVDS1#
As above, link1.
2nd LVDS2, 2nd LVDS2#
As above, link2.
2nd LVDS3, 2nd LVDS3#
As above, link2.
2nd LVDSCLK, 2nd LVDSCLK#
As above, clock link.
Single channel LVDS link is use the first channel only. Dual channel links, which are commonly used to transmit higher data rates, will use both the first and second channels.
The Txout3 and Txout3# for both first and second channels are not supported by the ETX CN700 board.

PIN NAME	LVDS SIGNAL	CHANNEL
1st LVDS0#	Txout0#	first
1st LVDS 0	Txout0	first
1st LVDS1#	Txout1#	first
1st LVDS 1	Txout1	first
1st LVDS2#	Txout2#	first
1st LVDS 2	Txout2	first
1st LVDS3#	Txout3#	first
1st LVDS 3	Txout32	first
1st LVDSCLK#	Txclock#	first
1st LVDSCLK	Txclock	first
2nd LVDS0#	Txout0#	second
2nd LVDS0	Txout0	second
2nd LVDS1#	Txout1#	second
2nd LVDS1	Txout1	second
2nd LVDS2#	Txout2#	second

2nd LVDS2#	Txout2	second
2nd LVDS3#	Txout3#	second
2nd LVDS3#	Txout3	second
2nd LVDSCLK#	Txclock#	second
2nd LVDSCLK	Txclock	second

BIASON
Controls panel contrast voltage.

DIGON
Controls panel digital power.
BLON#
Controls back-light power.
LTGIO0
General purpose I/O pin.
I2CLK, I2DAT
I2C interface for panel parameter EEPROM. This EEPROM is mounted on the LVDS receiver. The data in the EEPROM allows the ETX module to automatically set the proper timing parameters for a specific LCD panel.
DETECT#
Panel hot-plug detection. Implementation of this pin is optional. See the specific ETX module product manual for details.

LCD Interface Signals
NOTE: ETX modules may implement either this parallel interface or the LVDS flat panel interface described above. This pin implementation depends on which BCT-ETX-C3 variant is being used ie LVDS or LCD
R[0..5], G[0..5], B[0..5]
Parallel digital signals for red, green and blue pixel data.
LP(Line/Latch Pulse)
Horizontal Sync: This output supplies the horizontal synchronisation pulse for flat panels.
FLM (First Lime Marker)
This output supplies the vertical synchronisation pulse for flat panels.
DE
Data enable signal. Usage depends on display type.
SHCLK
Panel data clock signal.
DETECT#
Panel hot-plug detection.

Serial Port Signals
Note: that all serial port signals on the ETX module connectors are logic level signals. External transceiver devices are necessary for the conversion of the logic level signals to the desired physical interface such as RS232, RS422, or RS485.
DTR1#, DTR2#
Active-low data terminal ready outputs for the serial port. Handshake output signal notifies the modem that the UART is ready to establish a data communication link.
RI1#, RI2#
Active-low input is for the serial port. Handshake signals notify the UART when a telephone ring signal is detected by the modem.
TXD1, TXD2
Transmitter serial data output from serial port.
RXD1, RXD2
Receiver serial data input.
CTS1#, CTS2#
Active-low input for serial ports. Handshake signals notify the UART when the modem is ready to receive data.
RTS1#, RTS2#
Active-low output for serial port. Handshake signals notify the modem when the UART is ready to transmit data.
DCD1#, DCD2#
Active-low input for serial port. Handshake signals notify the UART when a carrier signal is detected by the modem.

DSR1#, DSR2#
This active-low input is for serial port. Handshake signals are use to notify the UART that the modem is ready to establish the communication link.

PS/2 Keyboard, PS/2 Mouse Signals
KBDAT
Bi-directional keyboard data signal.
KBCLK
Keyboard clock signal.
MSDAT
Bi-directional mouse data signal.
MSCLK
Mouse clock signal.
IRDA (SIR) Signals
IRTX, IRRX
Infrared transmit and receive pins.

Parallel Port Signals
The parallel port signals require external termination components. The parallel port has two alternative operating modes: parallel port and floppy disk. If the parallel port is used in parallel port mode, floppy disk support is not available via the parallel port. The LPT/FLPY# pin, which switches the parallel port modes, is sensed only at boot and cannot be changed dynamically. If simultaneous floppy drive and parallel support is needed, an external floppy controller may be incorporated in the baseboard design.
LPT/FLPY#
This ETX input signal selects whether the parallel port pins will implement parallel port or floppy support functionality. There is an internal pullup on this signal. If this signal is high or unconnected, the following parallel port pin functions are in effect:
STB#
This active-low signal is used to strobe the printer data into the printer.
AFD#
This active-low output tells the printer to automatically feed the next single line after each preceding line has been printed.
PD[0..7]
This bi-directional parallel data bus is used to transfer information between the CPU and the peripherals.
ERR#
This active-low signal indicates an error situation has occurred at the printer.
INIT#
This active-low signal is used to initiate the printer when low.
SLIN#
This active-low signal selects the printer.
ACK#
This active-low output from the printer indicates that it has received the previous data and that it is ready to receive new data.
BUSY#
This signal indicates that the printer is busy and not ready to receive new data.
PE
This signal indicates that the printer is out of paper.
SLCT#
This active-high output from the printer indicates that its power is on.

Floppy Signals
ETX modules support only a single floppy drive over the parallel port interface. When operating in floppy disk mode, the parallel port is not available. Note: ensure that the FDD cable has the necessary twist so it is recognised as Drive A:
LPT/FLPY#
This ETX input signal selects whether the parallel port pins will implement parallel port or floppy support functionality. There is an internal pullup on this signal. If this signal is low, the following floppy support functions are supported over the parallel port pins:
DENSEL
Indicates whether a low (250/300Kb/s) or high (500/1000Kbs) data rate has been selected.

INDEX#
This active-low Schmitt Trigger input signal is asserted by the disk drive when the diskette index hole is sensed.
TRK0#
This active-low Schmitt Trigger input signal is asserted by the disk drive when the head is positioned over the outermost track.
WP#
This active-low Schmitt Trigger input signal is asserted by the disk drive when a disk is write-protected.
RDATA#
The active-low, raw-data read signal from the disk drive. Each falling edge represents a flux transition of the encoded data.
DSKCHG#
This active-low input signal is asserted by the disk drive when the drive door has been opened.
DRV
This signal selects the floppy drive.
MOT
This active-low output activates the disk drive motor.
HDSEL#
This active-low output determines which disk drive head is active. Low = Head 0. High (open) = Head 1.
DIR#
This active-low output determines the direction of head movement (low = step-in, high = stepout).
STEP#
This active-low output signal is pulsed at a software-programmable rate to move the head during a seek operation.
WDATA#
This active-low output is a write pre-compensated serial data stream to be written onto the selected disk drive. Each falling edge causes a flux change on the media.
WGATE#
This active-low output enables the write circuitry of the selected disk drive.

Connector X4
IDE Signals
IDE signals are duplicated for the Primary and Secondary IDE channels. For each signal, the first signal name is for the primary channel and the second signal name is for the secondary channel.
PIDE_D0..15/ SIDE_D0..15
IDE Data Bus.
PIDE_A[0..2]/ SIDE_A[0..2]
IDE Address Bus.
PIDE_CS1#/ SIDE_CS1#
IDE Chip Select 1. This is the Chip Select 1 command output pin that enables the IDE device to watch the Read/Write Command.
PIDE_CS3#/ SIDE_CS3#
IDE Chip Select 3. This is the Chip Select 3 command output pin that enables the IDE device to watch the Read/Write Command.
PIDE_DRQ/ SIDE_DRQ
IDE DMA Request for IDE Master. This signal is asserted by an IDE device. It will be active-high in DMA or Ultra-33 mode and always be inactive-low in PIO mode.
PIDED_AK#/ SIDED_AK#
IDE DACK# for IDE Master. This signal grants the IDE DMA request to begin the IDE Master Transfer in DMA or Ultra-33 mode.
PIDE_RDY/ SIDE_RDY
IDE Ready. This is the input pin from the IDE Channel. It indicates that the IDE device is ready to terminate the IDE command in PIO mode. The IDE device can de-assert this input to expand the IDE command if the device is not ready. In Ultra-33 mode, this pin has different functions.
PIDE_IOR#/ SIDE_IOR#
IDE IOR# Command. This is the IOR# command output pin used to tell the IDE device to assert the Read Data in PIO and DMA mode. In Ultra-33 mode, this pin has different functions.

PIDE_IOW#/ SIDE_IOW#
IDE IOW# Command. This is the IOW# command output pin used to notify the IDE device that the available Write Data is already asserted by the IDE Busmaster in PIO and DMA mode. In Ultra-33 mode, this pin has different functions.
PIDE_INTRQ/ SIDE_INTRQ
Interrupt request signal from the IDE device.
HDRST#
Low-active hardware reset (RSTDRV inverted).

DASP_S
Time-multiplexed, open collector output that indicates that a drive is active. Also used for
Master/Slave negotiation on the Secondary IDE channel. If an IDE device such as a Flash Disk exists onboard the ETX module, this signal must be connected to the DASP_S pin of any other device connected to the Secondary IDE channel.
PDIAG_S
The signal is used for Master/Slave negotiation on the Secondary IDE channel. It is asserted by the Slave to indicate to a master that the slave has passed its internal Diagnostic command. If an IDE device such as a Flash Disk exists onboard the ETX module, this signal must be connected to the PDIAG_S pin of any other device connected to the Secondary IDE channel. This pin may additionally be used to detect the presence of the 80 conductor IDE cable which is required to support DMA66 or DMA100.
CBLID_P
On ETX modules that support DMA66 or DMA100, this pin may be used to detect the presence of an 80 conductor IDE cable on the primary IDE channel. This allows BIOS or system software to determine whether to enable high-speed transfer modes.

Ethernet Signals
The ETX Ethernet Interface is designed for use with an external 1:1/ 1:1 transformer.
TXD#, TXD (ANALOG TWISTED PAIR)
Ethernet Transmit Differential Pair. These pins transmit the serial bit stream on the Unshielded Twisted Pair (UTP) cable. The current-driven differential driver can be two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface to the Ethernet cable through an isolation transformer.
RXD#, RXD (ANALOG TWISTED PAIR)
Ethernet Receive Differential Pair. These pins receive the serial bit stream from the isolation transformer. The bit stream can be transmitted in either two-level (10BASE-T) or three-level (100BASE-TX) signals depending on the mode of operation. These signals interface to the Ethernet cable through an isolation transformer.
ACTLED/ LILED
The Activity LED pin indicates either transmitted or received data activity on the Ethernet port. This pin is asserted low when activity is detected. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.
The Link Integrity LED pin indicates link integrity. This pin is asserted low when the link is valid. It can sink 5mA to ground through an external LED and a limiting resistor to a 3.3V source.
These functions are combined on this pin
LILED/3V3VSUS
The Ethernet MAC on the ETX CN700 does not support a separate Link Function. This is provided on the ACTLED/LILED pin. Please connect this pin to the RJ45 Link LED via a current limiting resistor.
SPEEDLED
The Speed LED pin indicates high speed operation. This LED is not supported by all ETX boards. This pin is asserted low when a 100Mbps link is detected, and is not asserted for a 10Mbps link. It can sink 5mA to ground through an external LED and a current limiting resistor to a 3.3V source.

Ethernet Transformer Specification
Turns ratio transmit: 1:1 +/- 5%
Turns ratio receive: 1:1 +/- 5%
Insertion Loss 1 to 60 MHz: max. 1 dB
Return Loss 1 to 80 MHz: max. 10 dB
Common Mode Rejection
30 to 100 MHz: max. 30 dB
100 to 500 MHz: max. 20 dB
Cross Talk 1 to 80 MHz: max. 35 dB
Hi-Pot (Pri-Sec): min. 1500VRMS

Supported Ethernet transformer (examples):
Pulse H0002
Pulse H1012T

Power control signals
PWGIN
An active-high input to the ETX from an external power supply, indicating that the power is good and that the ETX can begin booting. Usage of this signal is not required because the ETX module contains its own power-good logic. The PWGIN signal can also be used as an active-low reset input to the ETX module.
5V_SB
Power input for the internal suspend and power control circuitry. Connect to a 5V, 100mA stand-by power source available. Should be connected to 5V supply if a standby supply is not available.
PS_ON
Active-low output from ETX module. Can be connected to the PS_ON input of an ATX power supply in order to switch the main output. In order for this pin to function, 5V_SB must be supplied to the ETX module.
PWRBTN#
Power Button Input. Connect to GND with momentary-contact switch or open collector driver to implement ATX power button control of PS_ON. [Note connecting this pin to ground for 4 seconds will cause immediate power off]. In order for this pin to function, 5V_SB must be supplied to the ETX module.
Power management signals
In order for these pins to function while VCC is powered down, 5V_SB must be supplied to the ETX module.
Note that these signals generally have pullup resistors to the suspend power supply inside the ETX module. Care must be taken in interfacing these signals to logic that is powered down when 5V_SB is active.
RSMRST#
Resume Reset input. This input may be driven low by external circuitry in order to reset the
power management logic on the ETX module.
SMBALRT#
System Management Bus Alert input. May be driven low by SMB devices in order to signal an event on the SM Bus.
BATLOW#
Battery low input. May be driven low by external circuitry to signal that the system battery is low, or may be used to signal some other external power management event.
GPE1#
General purpose power management event input 1. May be driven low by external circuitry to signal an external power management event. Within the ETX module, this pin is commonly connected to the chipset's LID# input.
GPE2#
General purpose power management event input 2. May be driven low by external circuitry to signal an external power management event. Within the ETX module, this pin is commonly connected to the chipset's RING# input.
EXTSMI
System management interrupt input. May be driven low by external circuitry to initiate an SMI.
Miscellaneous Signals
SPEAKER
PC speaker output signal. This logic-level signal can be connected to an external transistor in order to drive a piezoelectric or dynamic speaker.
BATT

3V backup cell input. BATT is typically connected to a 3V lithium backup cell for RTC operation and CMOS register non-volatility in the absence of system power. When RTC operation is not required by the application, some ETX modules can back up CMOS contents to EEPROM so a battery is not needed.

I2CLK, I2DAT

These clock and data lines implement an I2C-bus.which supports external slave devices only. Data rate is approximate 1-10kHz.. This interface is intended for support of EEPROMs and other simple I/O-devices

SMBDATA, SMBCLK

System Management Bus clock and data lines. May be used to support external SMBUS devices such as temperature and battery monitoring chips. The addresses of external SMBUS devices must be chosen so they do not conflict with addresses used internally on the ETX module.

KBINH

Keyboard Inhibit. Asserting this pin disables data input from the keyboard.

OVCR#

Over-current detect input. Used to monitor the USB power over-current. Pull with open collector to GND if over-current is detected.

Design Considerations

If you are considering designing your own host board, to accept the ETX CN700, then the first place to start is the ETX Specifications, which the latest level can be found at http://www.etx-ig.org/

As well as designing and manufacturing the ETX CN700, Blue Chip Technology can also provide assistance in the design of a custom host board. Contact Sales at the following address for more details

singleboardcomputer@bluechiptechnology.co.uk

The type of information that can be made available is as follows

- 3D Models, formats available Pro/E, .STP, .IGES
- Dimension Drawings, .DWG, .DXF
- BCT Eval Schematics, .PDF

When interfacing to the ETX CN700, the following considerations should be taken into account

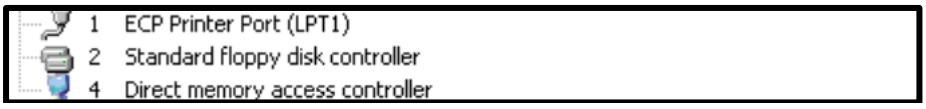
1/ only one FDD is supported as Drive A, so, when cabling from the HOST board, the FDD cable needs to have the necessary twist to distinguish it from Drive B

2/ For the Ethernet, the Link and Activity signals are shared

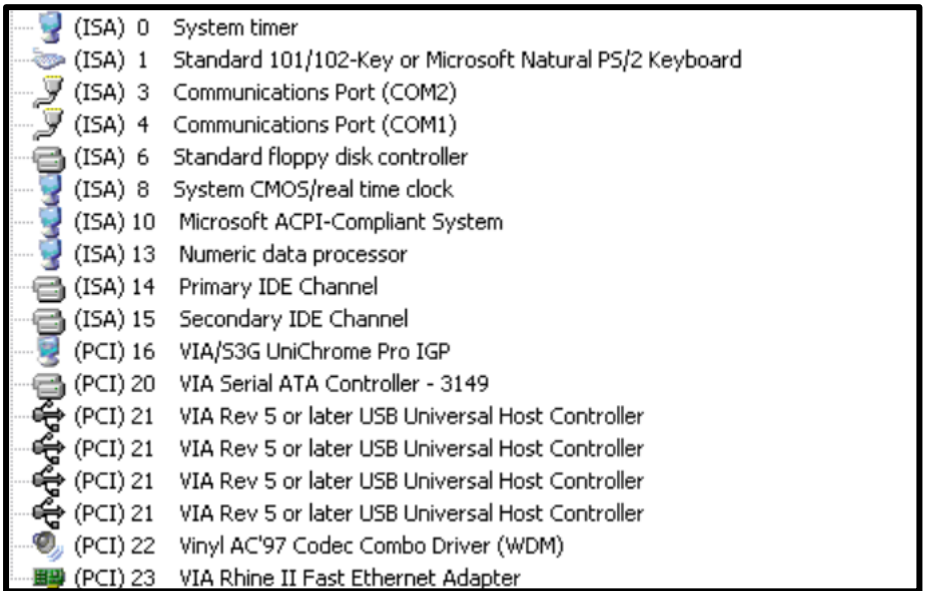
3/ Where ATX power supplies are being used; the 5V Standby voltage must be connected to the 5V voltage to allow operation

System Resources

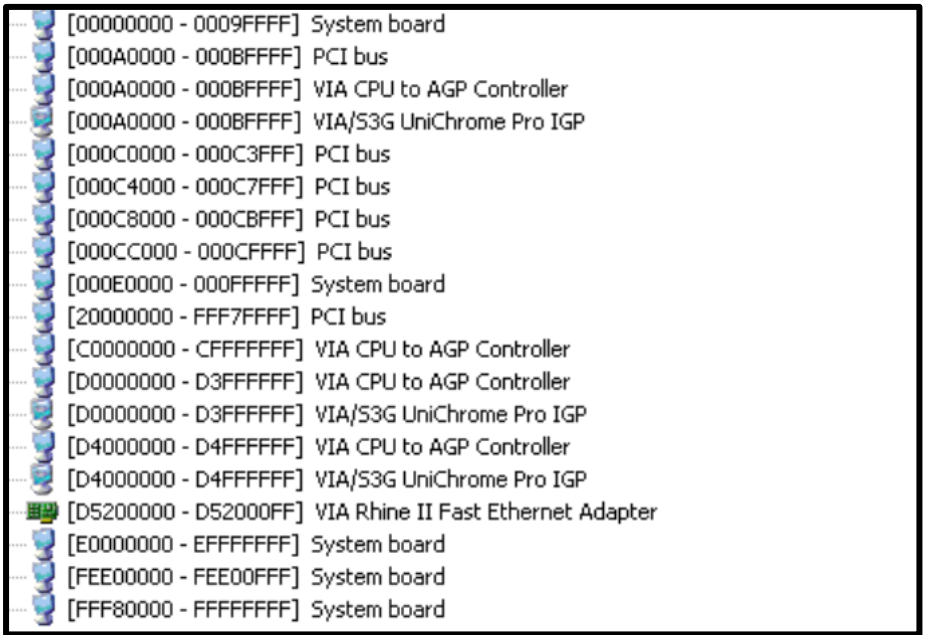
Direct Memory Access



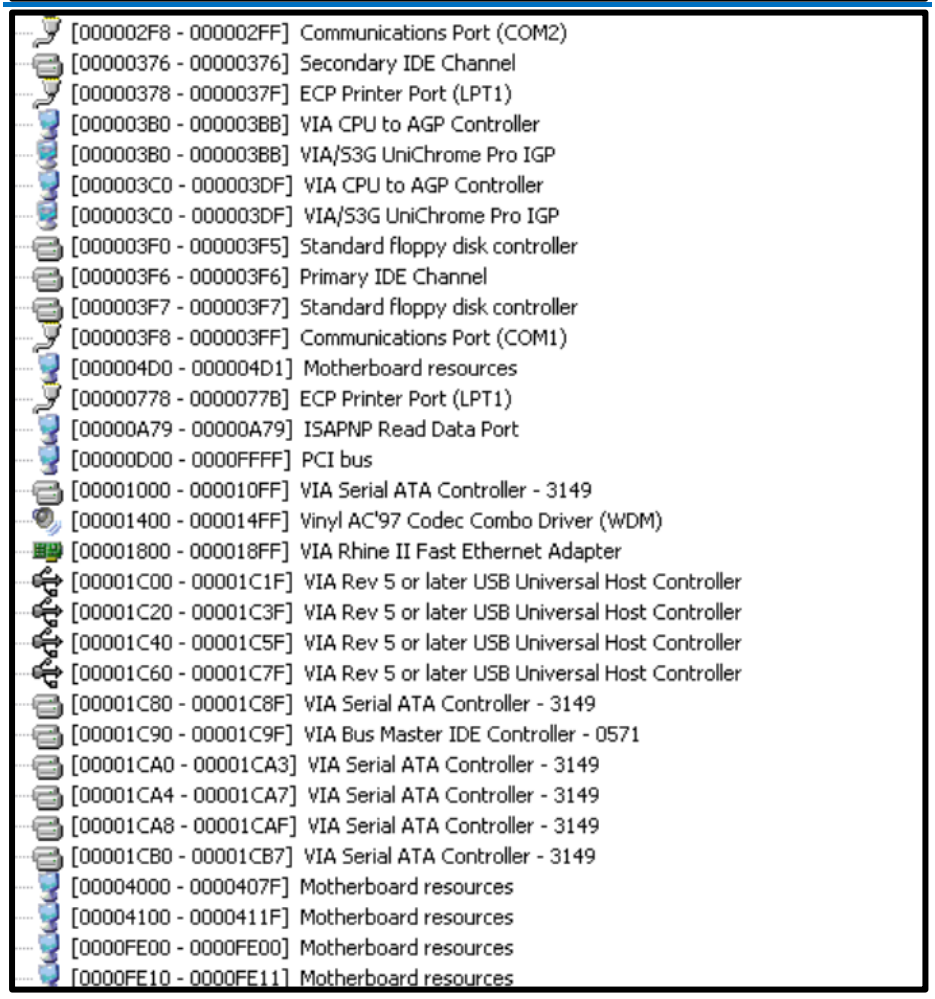
Interrupt Request



Memory



Input/Output



Maintenance

The ETX CN700 Single Board Computer should not require any regular maintenance. After a period of several years, it may be necessary to replace the battery, if present on the host carrier board, if it cannot maintain the CMOS clock whilst the AC power is disconnected.

Once fitted inside a System Unit, the servicing routine identified by the system manufacturer should be followed, this is typically to clean/exchange filter material and remove dust build up from within the casing

Amendment History

Issue Level	Issue Date	Author	Amendment Details
1.0	23-10-08	TMCK	First release
1.1	26-05-09	TMCK	Removed reference to 2Ghz CPU
1.2	28-08-09	TMCK	Added I/O,DMA, IRQ and Memory Maps
1.3		TMCK	Added Nano CPU, Signal Level definition on connectors
1.4	06-09-10	TMCK	Corrected LVDS3 pin definition on connector X3

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