

PIO-48d

**48 Channel Digital TTL
Input/Output Board**



User Manual

PIO-48d

User Manual

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INTRODUCTION

The PIO-48d is a PC-compatible short card which provides digital inputs and outputs.

There are 48 TTL-compatible programmable digital input/outputs available from the board. There are also three programmable timers. One of the timer outputs is available as an interrupt source or as a general purpose timekeeping device.

The input/output lines are available at an industry standard 50 way D-type connector.

ABOUT THE MANUAL

This manual is organised into four chapters, and two appendices. Each chapter covers a different aspect of using the PIO-48d. In order to get the best results from the product, the user is urged to read all chapters, paying particular note to Chapter 1 which deals with the initial installation of the card. The appendices may be used for reference at any time.

- Chapter 1** Explains how to configure the card to run in your computer via the user selectable links.
- Chapter 2** Details the connections to and from the card.
- Chapter 3** Gives details of the card's address mapping and internal register details allowing the user to write custom software to control the card.
- Chapter 4** Presents the card's technical specification. Use this section to determine the card's suitability for a particular application
- Appendix A** Gives a brief introduction to Binary and Hexadecimal numbering systems for those unfamiliar with the concepts.
- Appendix B** Lists the IBM-PC I/O address map and interrupt allocations and should be used along with Chapter 1 when first installing the card.

ELECTROMAGNETIC COMPATIBILITY (EMC)

This product meets the requirements of the European EMC Directive (89/336/EEC) and is eligible to bear the CE mark.

It has been assessed operating in a Blue Chip Technology Icon industrial PC. However, because the board can be installed in a variety of computers, certain conditions have to be applied to ensure that the compatibility is maintained. It meets the requirements for an industrial environment (Class A product) subject to those conditions.

- The board must be installed in a computer system which provides screening suitable for the industrial environment.
- Any recommendations made by the computer system manufacturer/supplier must be complied with regarding earthing and the installation of boards.
- The board must be installed with the backplate securely screwed to the chassis of the computer to ensure good metal-to-metal (i.e. earth) contact.
- Most EMC problems are caused by the external cabling to boards. It is imperative that any external cabling to the board is totally screened, and that the screen of the cable connects to the metal end bracket of the board and hence to earth. It is recommended that round screened cables with a braided wire screen are used in preference to those with a foil screen and drain wire. Use metal connector shells which connect around the full circumference of the screen; they are far superior to those which earth the screen by a simple “pig-tail”. Standard ribbon cable will not be adequate unless it is contained wholly within the cabinetry housing the industrial PC.
- Ensure that the screen of the external cable is bonded to a good RF earth at the remote end of the cable.

- Cables which connect externally to boards at TTL levels should not exceed two metres in length. This restriction does not apply to opto-isolated boards.

Failure to observe these recommendations may invalidate the EMC compliance.

Warning

This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

EMC Specification

A Blue Chip Technology Icon industrial PC fitted with this card meets the following specification:

Emissions: EN 55022:1995

Radiated	Class A
Conducted	Class A & B

Immunity: pr EN 50082-2:1991 incorporating:

Electrostatic Discharge	IEC 801-2:1984 Performance Criteria A
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Radio Frequency Susceptibility	IEC 801-3:1984 Performance Criteria A
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Fast Burst Transients	IEC 801-4:1988 Performance Criteria A
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CHAPTER 1

Installing the PIO-48D

Before installing the card into your computer system, there are a number of user-configurable links that must be set.

The positioning of these links will depend upon the computer system into which the card is being fitted. Before fitting any links please read the following section.

If you are unfamiliar with binary and hexadecimal numbering systems a primer is included in the appendix.

Base Address

For correct communication between the card and the host computer, the range of addresses that the card will occupy must be set. The base address represents the first address that the card will use. The PIO-48d requires a total of 12 contiguous addresses (including the base address) for correct operation. All Blue Chip Technology cards are factory set to a default base address of 300 hex. Check to ensure that the base address and the full range of addresses are free for use.

If the addresses are not free another range must be chosen. As a guide, please use the information contained in the appendix to assist in choosing a suitable base address.

If you are not sure refer to your computer system handbook for information relating to other peripheral devices possibly already installed (additional communications cards, parallel ports or games ports etc.).

If the addresses are available for use then proceed as follows:-

- Locate the row of header pins (JP2). These pins are marked “SET BASE ADDR.” and start with the pair of pins marked with an arrow. This pair of pins represents the lowest single base address selection.
- Subsequent pins represent addresses of increasing size. The highest single base address link is hex 200.
- To select an address, a link position must be left open. Placing a link on a pair of pins de-selects that particular address.

Example:

To select a base address of 300 hex, the links should be set as follows:-

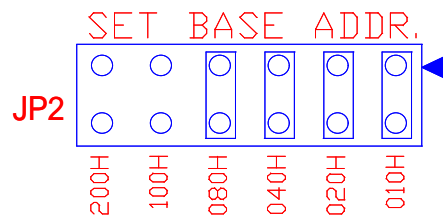


Figure 1 Example Base Address Selection

Interrupt Selection

As part of the link between the PIO-48d and the host computer, an interrupt signal may be set to occur at regular intervals from the timer or when an input changes state. The application software then uses the interrupt to service the calling device. The use of interrupts is not essential but greatly enhances the functionality of the card.

In order to use interrupts for data transfer, the user must select an Interrupt Request Channel (IRQ) for the card to use. The PIO-48d can use any one of Interrupt Channels IRQ-2 to -7.

As with the selection of a base address, the chosen Interrupt Channel must be free for use and not be selected by any other peripheral in the system. The appendix may be used to identify the Interrupt Channels that are normally already in use by most systems and which ones will probably be free for use.

Check that the selected channel is free for use.

If you are not sure refer to your computer system handbook for information relating to other peripheral devices possibly already installed (additional communications cards, parallel ports or games ports etc.).

If the chosen channel is available for use by the PIO-48d, set the card as follows:-

- Locate the row of header pins labelled JP1. These pins are marked "SET IRQ".
- To select an interrupt place a link on the pair of pins corresponding to the chosen Interrupt Request Channel. All other pins must be left open.

Example: To select an Interrupt Request of IRQ-5, set the links as follows:-

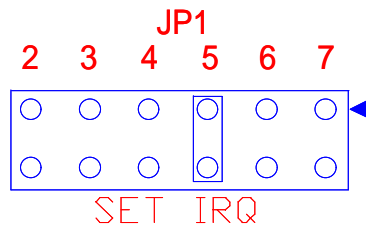


Figure 2 Example Interrupt Request Selection

Further Interrupt Options

The source of the interrupt signal is also a user selectable option. An interrupt may be selected from either an external user input or from the on-board timer using the jumper block JP3.

When the external input option is selected (“PIO”), the interrupt can be used to flag the occurrence of an outside event.

When the on-board timer is selected as the source (“TIMER”), the timer acts as a clock to provide regular timed interrupts. The time period of the interrupts can be programmed in software.

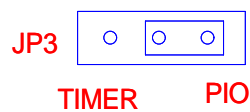


Figure 3 Example Interrupt Source Selection

CHAPTER 2

Connection Details

The following table refers to the 50 way D-type plug at the rear of the card.

PIN	USAGE	PIN	USAGE	PIN	USAGE
1	PIO1 port A, bit 0	18	PIO1 port C, bit 1	34	PIO2 port B, bit 1
2	PIO1 port A, bit 1	19	PIO1 port C, bit 2	35	PIO2 port B, bit 2
3	PIO1 port A, bit 2	20	PIO1 port C, bit 3 and/or Interrupt Input	36	PIO2 port B, bit 3
4	PIO1 port A, bit 3	21	PIO1 port C, bit 4	37	PIO2 port B, bit 4
5	PIO1 port A, bit 4	22	PIO1 port C, bit 5	38	PIO2 port B, bit 5
6	PIO1 port A, bit 5	23	PIO1 port C, bit 6	39	PIO2 port B, bit 6
7	PIO1 port A, bit 6	24	PIO1 port C, bit 7	40	PIO2 port B, bit 7
8	PIO1 port A, bit 7	25	PIO2 port A, bit 0	41	PIO2 port C, bit 0
9	PIO1 port B, bit 0	26	PIO2 port A, bit 1	42	PIO2 port C, bit 1
10	PIO1 port B, bit 1	27	PIO2 port A, bit 2	43	PIO2 port C, bit 2
11	PIO1 port B, bit 2	28	PIO2 port A, bit 3	44	PIO2 port C, bit 3
12	PIO1 port B, bit 3	29	PIO2 port A, bit 4	45	PIO2 port C, bit 4
13	PIO1 port B, bit 4	30	PIO2 port A, bit 5	46	PIO2 port C, bit 5
14	PIO1 port B, bit 5	31	PIO2 port A, bit 6	47	PIO2 port C, bit 6
15	PIO1 port B, bit 6	32	PIO2 port A, bit 7	48	PIO2 port C, bit 7
16	PIO1 port B, bit 7	33	PIO2 port B, bit 0	49	Digital Ground
17	PIO1 port C, bit 0 and/or Interrupt Input			50	External Clock - Timer 2 Input

Driving the Timer from External Sources

The on-board timer contains three independent 16-bit counter sections which may be programmed to various count lengths and modes of operation. The first two timers (Timer 0 and Timer 1) are cascaded. All three timers may provide the interrupt source.

The third timer however has its clock input connected to the 50 way D-type connector and is therefore available for the user to provide an external clock input. The external clock must be in the range 0 volts to +5 volts with a maximum frequency of 10MHz.

Suitable Signal Types

The input and output signals for the PIO-48d are strictly digital TTL levels with voltage limits of zero volts for a logic low and +5 volts for a logic high. Voltages outside these limits may cause damage to the card. The output current drive capability makes the card suitable for connection to TTL logic type circuits. The PIO-48d is compatible with most types of TTL logic. Because the lines are TTL it is recommended that input signal lines do not exceed 2 metres in length. Operation at longer lengths may cause drive level problems.

Driving conventional relay coils is not recommended without external protection even if the coil current required is less than the PIO-48d can provide. Relay coils are 'inductive' and as such can generate large voltages when energized and de-energized. These will destroy the outputs.

CHAPTER 3

Programming Details

This chapter provides details of the cards internal registers.

The board's input / output facilities are provided by two NEC μ PD71055 PIO devices (compatible with Intel I8255) and an NEC μ PD71054 Timer (compatible with the Intel i8254).

Each PIO provides 24 programmable digital I/O channels. It is suitable for sensing the presence of, or driving TTL connections only. These connections should be kept as short as possible, less than 2 metres is recommended.

Each PIO appears to the PC as four ports. The first three can be set as input or output by writing suitable codes to the fourth Control Port. These are accessed at the addresses shown in the map below.

A summary of the codes required to change the operation of the ports are given later. A typical sequence of events to use this feature would be :

- Decide on the mix of input/outputs required and write the appropriate code to the Control Register.
- Read from the selected output port or write to the selected output port.

Address Map

The address map for the PIO-48d occupies a 16-byte block of which the first 12 addresses are used.

ADDRESS	FUNCTION	READ/ WRITE
Base + 0	PIO 1, Port A Input/Output Register (Channel 0 to 7)	R/W
Base + 1	PIO 1, Port B Input/Output Register (Channel 8 to 15)	R/W
Base + 2	PIO 1, Port C Input/Output Register (Channel 16 to 23)	R/W
Base + 3	PIO 1, Control Register	W
Base + 4	PIO 2, Port A Input/Output Register (Channel 24 to 31)	R/W
Base + 5	PIO 2, Port B Input/Output Register (Channel 32 to 39)	R/W
Base + 6	PIO 2, Port C Input/Output Register (Channel 40 to 47)	R/W
Base + 7	PIO 2, Control Register	W
Base + 8	Timer 0 Count Register	R/W
Base + 9	Timer 1 Count Register	R/W
Base + 10	Timer 2 Count Register	R/W
Base + 11	Timer Control Register	W

The μ PD71055 PIO and μ PD71054 Timer ICs are complex devices. For full details on how to program these devices, refer to the manufacturer's data sheets. Presented here is a brief summary of the main features of each.

μPD71055 PIO

The μPD71055 PIO chip can operate in one of three modes.

The first (Mode 0) provides for simple inputs and outputs for three, 8 bit ports. Data is written to or read from a specified port (A, B, or C) without the use of handshaking. The following table gives a summary of the most commonly used control words which must be written to the control port to configure the μPD71055 I/O ports in Mode 0.

CONTROL WORD (hex)	CONTROL WORD (decimal)	SET ALL of PORT A as	SET ALL of PORT B as	SET HIGH 4 BITS of C as	SET LOW 4 BITS of C as
80	128	Output	Output	Output	Output
81	129	Output	Output	Output	Input
82	130	Output	Input	Output	Output
83	131	Output	Input	Output	Input
88	136	Output	Output	Input	Output
89	137	Output	Output	Input	Input
8A	138	Output	Input	Input	Output
8B	139	Output	Input	Input	Input
90	144	Input	Output	Output	Output
91	145	Input	Output	Output	Input
92	146	Input	Input	Output	Output
93	147	Input	Input	Output	Input
98	152	Input	Output	Input	Output
99	153	Input	Output	Input	Input
9A	154	Input	Input	Input	Output
9B	155	Input	Input	Input	Input

Mode 1 enables the transfer of data to or from a specified 8 bit port (A or B) in conjunction with strobes or handshaking signals on port C.

In Mode 2, data is transferred via one bi-directional 8 bit port (A) with handshaking (port C).

Refer to the μPD71055 or i8255 data sheet for full details of the settings and use of Modes 1 and 2.

µPD71054 Timer

The µPD71054 Timer circuit contains three independent 16-bit counters which may be operated in a variety of modes. There are five basic modes of operation with each mode providing a different output signal. Presented here is a brief summary of some of the modes possible by programming the timer's internal registers.

On the PIO-48d, Timer 0 and Timer 1 are connected in series to provide the facility of a long delay period.

Timer 2 is independent and has to be clocked from an external input.

The outputs from Timer 1 and Timer 2 are logically combined to allow interrupt generation.

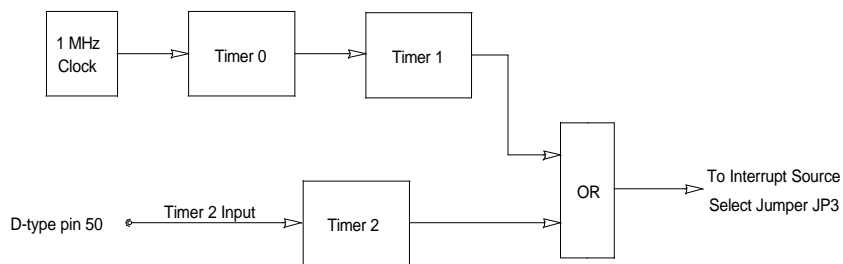


Figure 4 Block Diagram of Timer Connections

Timer Modes

The following modes of operation exist by programming the control register within the μ PD71054. Please note that not all are possible with the PIO-48d.

Mode 0

When programmed, the output pin will go LOW. When the counter decrements from the value loaded into the count registers to zero, the output pin will go HIGH. It will remain high until the count is re-programmed into the count registers.

Mode 1

When the count registers are programmed the output pin will be HIGH. When a LOW going signal is applied to the gate input, the count starts and the output will fall LOW, returning HIGH at the end of the count. This mode is not available on the PIO-48d because the timer gate lines are held at +5 volts.

Mode 2

This mode operates as a frequency divider. When programmed the output pin is HIGH. When the count decrements to a value of 1 the output pin will go LOW for ONE clock cycle only and then return HIGH. This cycle repeats continuously without the need to re-program the count value.

Mode 3

When programmed the output pin will toggle each time the count register decrements to its base level from the value programmed into it. If the count value loaded is an odd number then the counter will reach zero before the output pin toggles. This mode therefore acts as a frequency divider with an approximate 1:1 mark-space ratio.

Mode 4

This mode is similar to mode 2 but the output pin pulses when the count reaches zero instead of 1.

Mode 5

This mode is similar to mode 4 except that the count sequence is triggered by the gate line. As with mode 1, this mode is not available since the timer gate lines are held at +5 volts.

CHAPTER 4

Technical Specifications

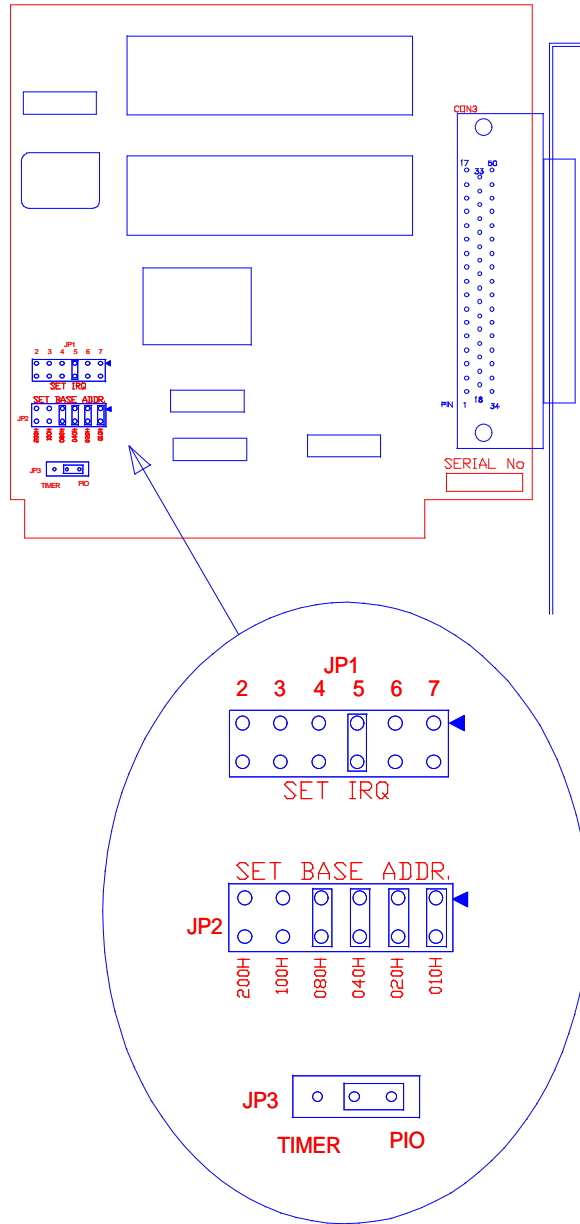
Number Of I/O Channels:	48 arranged as 2 x 3 x 8 I/O bits
Signal Levels:	5 Volt TTL Logic Levels
Outputs:	
Logic Low Level:	0 Volts (min.) - 0.6 Volts (max.)
Logic High Level:	4 Volts (min.) - 5 Volts (max.)
Output Drive Current:	2.5 mA (Logic Low) Vout = 0.4 Volts -400 μ A (Logic High) Vout = 3.5 Volts
Input Loading:	-10 μ A (Logic Low) +10 μ A (Logic High)
Timers:	3 x 16 Bit. Timers 0 and 1 cascaded to provide interrupt source with a time interval programmable from 1 μ s to 71.5 mins. Timer 2 externally clocked also providing interrupt source. Minimum time period 200ns, maximum time period unlimited.
Interrupt Sources:	Link selectable between Timer and an event on digital I/O lines DIO-16 or DIO-19.
Interrupt Levels Supported:	IRQ-2, -3, -4, -5, -6, -7
Address Overhead:	12 contiguous addresses in 16 byte block

Board Power Requirement: +5 Volts, 550 mW maximum

Signal Connections: 1 x 50 way male 'D-type' plug

Dimensions: 107 (L) x 107 (H) board only
121 (L) x 127 (H) x 22 (W) including bracket

PCB Layout Diagram



APPENDIX A - NUMBERING SYSTEMS

Binary and Hexadecimal Numbers

The normal numbering system is termed DECIMAL because there are ten possible digits (0 to 9) in any single column of numbers. Decimal numbers are also referred to as numbers having a Base 10. When counting, the numbers increment in the units column from 0 up to 9. The next increment resets the units column to 0 and carries over 1 into the next column. This 1 indicates that there has been a full ten (the base number) counts in the units column. The second column is therefore termed the “tens” column.

It is more convenient when programming to use a number system that provides a clearer picture of the hardware at an operational or register level. The two most common number systems used are BINARY and HEXADECIMAL. These two systems provide an alternative representation to decimal numbers.

For a binary number there are only 2 possible values (0 or 1) and as a result binary numbering is often known as Base 2. When counting in binary numbers, the number increments the units column from 0 to 1. At the next increment the units column is reset to 0 and 1 is carried over to the next column. This column indicates that a full two counts have occurred in the units column. Now the second column is termed the “twos” column.

Hexadecimal numbers may have 16 values (0 to 9 followed by the letters A to F). It is also known as a system with the Base 16. With this counting system the units increment from 0 to 9 as with the decimal system, but at the next count the units column increments from 9 to A and then B, C and so on up to F. After F the units column resets to 0 and the next column increments from 0 to 1. This 1 indicates that sixteen counts have occurred in the units column. The second column is termed the “sixteen’s” column.

The following table shows how the three systems indicate successive numbers

Decimal Base 10	Binary Base 2	Hexadecimal Base 16
0 0	0 0 0 0 0	0 0
0 1	0 0 0 0 1	0 1
0 2	0 0 0 1 0	0 2
0 3	0 0 0 1 1	0 3
0 4	0 0 1 0 0	0 4
0 5	0 0 1 0 1	0 5
0 6	0 0 1 1 0	0 6
0 7	0 0 1 1 1	0 7
0 8	0 1 0 0 0	0 8
0 9	0 1 0 0 1	0 9
1 0	0 1 0 1 0	0 A
1 1	0 1 0 1 1	0 B
1 2	0 1 1 0 0	0 C
1 3	0 1 1 0 1	0 D
1 4	0 1 1 1 0	0 E
1 5	0 1 1 1 1	0 F
1 6	1 0 0 0 0	1 0
1 7	1 0 0 0 1	1 1
1 8	1 0 0 1 0	1 2
1 9	1 0 0 1 1	1 3
2 0	1 0 1 0 0	1 4

Notice how the next higher column does not increment until the lesser one to its right has overflowed.

Binary representation is ideally suited where a visual representation of a computer register or data is needed. Each column is termed a **BIT** (from **B**inary **digIT**). Only five bits are shown in the above table. With larger numbers, more bits are required. Normally bits are arranged in groups of eight termed **BYTES**. By definition there are 8 **BITS** per **BYTE**. Each bit (or column) has a value. In the binary table above the rightmost or least significant column each digit has a value of 1. Each digit in the next column has a value of 2, the next 4, then 8 and so on.

The following diagram illustrates this.

BIT No	7	6	5	4	3	2	1	0
DECIMAL VALUE	128	64	32	16	8	4	2	1

To determine the decimal value of a binary pattern, add up the decimal number of each column containing a binary “1”.

BIT No	7	6	5	4	3	2	1	0
DECIMAL VALUE	128	64	32	16	8	4	2	1
BINARY NUMBER	1	1	0	0	0	1	1	0

The above example shows the binary pattern that is equivalent to 198_{Decimal}.

The binary string defining a Byte can be unwieldy. To make it less error prone, the 8 bits forming a byte are divided into two groups of 4 bits, known as NIBBLES. With four bits there are 16 possible numeric combinations (including zero). A convenient method of representing each nibble is to use the hexadecimal base 16 system.

When converting binary to hex, the byte is divided into nibbles each represented by a single hex digit. This technique is applied to the selection of the base address for the circuit board. The following diagram illustrates the construction of a hex number.

BIT No	7	6	5	4	3	2	1	0
NIBBLE VALUE	8	4	2	1	8	4	2	1
BINARY NUMBER	1	1	0	0	0	1	1	0

AAAAAAAAAAAAU AAAAAAAAAAAU

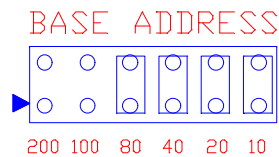
HEXADECIMAL: C 6

$$\begin{aligned} \text{Hexadecimal upper nibble} &= (1 \times 8) + (1 \times 4) + (0 \times 2) + (0 \times 1) = 12 \\ \text{lower nibble} &= (0 \times 8) + (1 \times 4) + (1 \times 2) + (0 \times 1) = 6 \end{aligned}$$

The resulting value is C6_{Hex}, since 12_{Decimal} equals C_{Hex}.

Base Address Selection

Each column can be physically represented on the board by a pair of pins. In practice, the boards cover a range of addresses (usually 16_{Decimal}). Therefore the low order four bits are not included, but two higher order bits are added. This gives an address range of 0 to 3F0_{Hex}. The following diagram shows a typical set of pins.



Here a link is fitted to denote a binary or logic “0”, or left open to indicate a binary or logic “1”. The example shows a base address setting of 300_{Hex}.

APPENDIX B - PC MAPS

PC/XT/AT I/O Address Map

<u>Address</u>	<u>Allocated to:</u>
000-01F	DMA Controller 1 (8237A-5)
020-03F	Interrupt Controller 1 (8259A)
040-05F	Timer (8254)
060-06F	Keyboard Controller (8742) Control Port B
070-07F	RTC and CMOS RAM, NMI Mask (Write)
080-09F	DMA Page Register (Memory Mapper)
0A0-0BF	Interrupt Controller 2 (8259)
0F0	Clear NPX (80287) Busy
0F1	Reset NPX (80287)
0F8-0FF	Numeric Processor Extension (80287)
1F0-1F8	Hard Disk Drive Controller
200-207	Reserved
278-27F	Reserved for Parallel Printer Port 2
2F8-2FF	Reserved for Serial Port 2
300-31F	Reserved
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	Reserved for SDLC Communications, Bisync 2
3A0-3AF	Reserved for Bisync 1
3B0-3BF	Reserved
3C0-3CF	Reserved
3D0-3DF	Display Controller
3F0-3F7	Diskette Drive Controller
3F8-3FF	Serial Port 1

PC/XT Interrupt Map

<u>Number</u>	<u>Allocated to:</u>
NMI	Parity
0	Timer
1	Keyboard
2	Reserved
3	Asynchronous Communications (Secondary) SDLC Communications
4	Asynchronous Communications (Primary) SDLC Communications
5	Fixed Disk
6	Diskette
7	Parallel Printer

PC/AT Interrupt Map

<u>Level</u>	<u>Allocated to:</u>
CPU NMI	Parity or I/O Channel Check
CTLR 1	CTLR 2 (Interrupt Controllers)
IRQ 0	Timer Output 0
IRQ 1	Keyboard (Output Buffer Full)
IRQ 2	Interrupt from CTLR 2
	IRQ 8 Real-time Clock Interrupt
	IRQ 9 S/w Redirected to INT 0AH (IRQ 2)
	IRQ 10 Reserved
	IRQ 11 Reserved
	IRQ 12 Reserved
	IRQ 13 Co-processor
	IRQ 14 Fixed Disk Controller
	IRQ 15 Reserved
IRQ 3	Serial Port 2
IRQ 4	Serial Port 1
IRQ 5	Parallel Port 2
IRQ 6	Diskette Controller
IRQ 7	Parallel Port 1

DMA Channels

0	Memory Refresh
1	Spare
2	Floppy Disk Drive
3	Spare