DIO-32d

Digital Input/Output Card

User Manual

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INTRODUCTION

The DIO-32d is a compatible short card which provides the user with 16 digital inputs and 16 digital outputs, all of which are opto-isolated from the host computer ground system.

The card features an isolated 24 volt supply, an on-board timer and user selectable base address, interrupt source and interrupt level.

The timer may be used as an interrupt source or as a general purpose timekeeping device.

ABOUT THE MANUAL

This manual is organised into four chapters and two appendices. Each chapter covers a different aspect of using the DIO-32d. In order to get the best results from the product, the user is urged to read all chapters, paying particular note to Chapter 1 which deals with the initial installation of the card. The appendices may be used for reference at any time.

Chapter 1	Explaines how to configure the card to run in your computer via the user selectable links.
Chapter 2	Details the connections to and from the card.
Chapter 3	Gives details of the card's address mapping and internal register details allowing the user to write custom software to control the card.
Chapter 4	Details the card's technical specification. Use this section to determine the card's suitability for a particular application.
Appendix A	Gives a brief introduction to Binary and Hexadecimal numbering systems for those unfamiliar with the concepts.
Appendix B	Lists the IBM-PC I/O address map, interrupt and DMA allocations and should be used along with Chapter 1 when first installing the card.

CHAPTER 1

Installing the DIO-32d

Before installing the card into your computer system, there are a number of user-configurable links that must be set.

The positioning of these links will depend upon the computer system into which the card is being fitted. Before fitting any links to the card, please read the next section.

If you are unfamiliar with binary and hexadecimal number systems a primer is included in the appendix.

Base Address

For correct operation of the card in the host computer, the range of addresses that the card will occupy must be set. The base address represents the first address that the card will use. The DIO-32d requires a total of 12 contiguous addresses (including the base address) for correct operation. All Blue Chip Technology cards are factory set to a default base address of 300 hex. Check to ensure that the base address and the full range of addresses are free of use.

If the addresses are not free another range must be chosen. As a guide, please use the information contained in the appendix to assist in choosing a suitable base address.

If you are not sure, refer to your computer system handbook for information relating to other peripheral devices possibly already installed (additional communications cards, parallel ports or games ports etc.).

If the addresses are available for use then proceed as follows:

- Locate the row of header pins (JP3). These pins are marked “BASE ADDRESS”. Each pair of pins represents a binary digit starting with the pair of pins marked with an arrow. This pair of pins represents the lowest hex value (008 hex), subsequent pins represent increasing values. The highest single base address link is 200 hex.

- To select an address, a link position must be left open. Placing a link on a pair of pins de-selects that particular address.

Example:

To select a base address of 300 hex, the links should be set as follows:

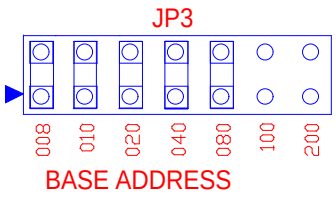


Figure 1 Example Base Address Selection

Interrupt Selection

As part of the link between the DIO-32d and the host computer, an interrupt signal may be set to occur at regular intervals from the timer or when an input changes state. The application software then uses the interrupt to service the calling device. The use of interrupts is not essential but greatly enhances the functionality of the card.

In order to use interrupts for data transfer, the user must select an Interrupt Request Channel (IRQ) for the card to use. The DIO-32d can use any one of Interrupt Channels IRQ-2 to -7.

As with the selection of base addresses, the chosen Interrupt Channel must be free for use and not be selected by any other peripheral in the system. The Appendix may be used to identify the Interrupt Channels that are normally already in use by most systems and which ones will probably be free for use.

Check that the selected channel is free for use.

If you are not sure, refer to your computer system handbook for information relating to other peripheral devices possibly already installed (additional communications cards, parallel ports or games ports etc.).

If the Interrupt Channel chosen is available for use by the DIO-32d then set the card as follows:

- Locate the row header pins labelled JP4. These pins are marked “SET INTERRUPT”.

- To select an interrupt place a link on the pair of pins corresponding to the chosen Interrupt Request Channel. Only one channel should be selected, all other pins must be left open.

Example:

To select an Interrupt channel of 5, the links should be set as follows:

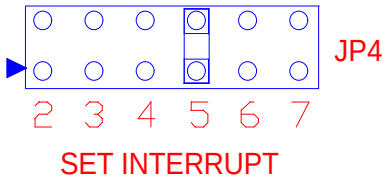


Figure 2 Example Interrupt Signal Selection

Further Interrupt Options

The on-board timer contains three independent 16 bit counter/timer sections which may be programmed to various count lengths and modes of operation.

The source of the interrupt signal is also an user option, selectable by jumper JP1. An interrupt source may be selected from either Timer 1 or Timer 2.

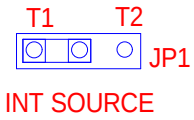


Figure 3 Example Interrupt Source Selection

The first two timers (Timer 0 and Timer 1) are cascaded. The timer period of the interrupts is programmed via software.

For Timers 0 and 1 the minimum delay is 2 microseconds and the maximum delay is 65,535 microseconds. For Timer 2 the minimum and maximum time delays are 2 microseconds and 71.58 minutes respectively.

To calculate the counter setting divide the required delay by the timer master clock period (in this case 1 microsecond). For example if a delay of 10 microseconds is required then:

10µ / 1µs = 10,000 counts.

Driving the Timer from External Sources

Timers 1 and 2 may provide the interrupt source. Whilst Timer 0 is driven by the on-board oscillator, the clock input for Timer 2 is available at the 50 way 'D' connector, for the user to provide an external clock input.

The external clock input is selectable. It may share the same signal pin as digital input 1 (DIN-1, which is a differential input), or use a dedicated (single-ended) input pin. The selection is by the setting of jumper JP22. JP22 is a 3-pin header. If the centre pin is connected to pin "A", the digital input 1 (DIN-1) is the input. If pin "B" is connected, the clock input is selected as the source.

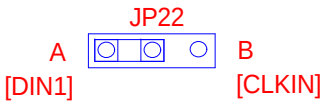


Figure 4 Timer 2 Clock Source Selection Jumper

The external clock must be in the range 0 to +5 volts with a maximum frequency of 10MHz.

Maximum Input Voltage Range

The DIO-32d allows a maximum input of 24 volts. Although the range is set at 24 volts, the opto-isolators will actually work at considerably lower voltages than the set range. Since opto-isolators are not strictly digital devices they will allow switching at these lower levels. The minimum recommended voltage for the input is 3 volts and the maximum level is 24 volts.

Voltages greater than 24 volts on any input will damage the card.

Selecting the Output Voltage Source

Because the digital outputs from the DIO-32d are open collector types, a load must be placed between the output terminal and a positive voltage supply. This may be either an external supply, or an isolated +24 volt supply on-board supply. The link JP13 selects which supply is to be used.

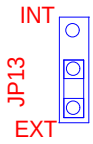


Figure 5 The Output Power Supply Selection Jumper

The internal 24 volt source is protected by a 125mA fuse which will fail if excessive load currents are drawn. This will occur if an output is shorted to ground or if the load resistance's used are too low in value. The internal supply can provide up to 42mA in total (approx. 2½MA per channel is all channels are used). If an external supply is used then the maximum current per channel increases to 500mA. The output devices are also protected by a 125mA fuse.

Other Links

Some boards are supplied with an additional set of links fitted (JP5 to JP12 and JP14 to JP21). These are not used and should be left open.

CHAPTER 2

Connection Details

The following table refers to the 50 way 'D' plug at the rear of the card. Pin1 of the connector is at the bottom left when looking 'into' the pins of the connector.

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	+DIN1 (+T2 I/P)	18	-DIN9	34	DOUT2
2	-DIN1 (-T2 I/P)	19	+DIN10	35	DOUT3
3	+DIN2	20	-DIN10	36	DOUT4
4	-DIN2	21	+DIN11	37	DOUT5
5	+DIN3	22	-DIN11	38	DOUT6
6	-DIN3	23	+DIN12	39	DOUT7
7	+DIN4	24	-DIN12	40	DOUT8
8	-DIN4	25	+DIN13	41	DOUT9
9	+DIN5	26	-DIN13	42	DOUT10
10	-DIN5	27	+DIN14	43	DOUT11
11	+DIN6	28	-DIN14	44	DOUT12
12	-DIN6	29	+DIN15	45	DOUT13
13	+DIN7	30	INTERNAL +24V	46	DOUT14
14	-DIN7	31	+DIN16	47	DOUT15
15	+DIN8	32	+T2 TIMER I/P	48	DOUT16
16	-DIN8	33	DOUT 1	49	EXTERNAL +24V
17	+DIN9			50	COMMON GND

Digital Inputs

The input signals for the DIO-32d are digital with voltage limits of zero volts for a logic low and up to +24 volts for a logic high. Voltages outside these limits may cause damage to the card.

Digital inputs on channels 1 to 14 (DIN1-14) are isolated from the PC power supplies and also from each other. The signals are applied between the "+DIN" and "-DIN" connections.

Input channels 15 and 16 (DIN15 & 1) share a common connection, the signals must be applied between "+DIN" and "COMMON GND".

Digital Outputs

The digital outputs are open collector types and must be returned to a positive supply voltage by a load. The positive supply may be either the on-board 24 volts supply or an externally provided source of not greater than 24 volts.

When an output is switched "on" then the voltage at the collector output will be at a logic low. The output voltage for this logic level is typically 0.7 volts.

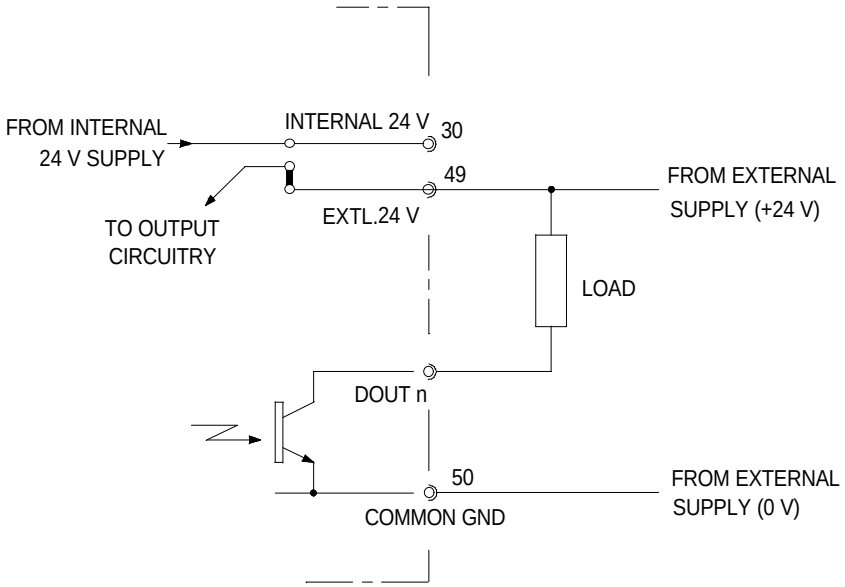


Figure 6 Showing the Dio-32d Output Connections

The voltage at the collector output will range from 0.7V for a logic low up to a value equal to the supplied rail voltage. When an output transistor is switched on, the maximum permissible current sink is 500mA.

Note that it is the maximum POWER dissipation of each collector output that determines the limits of operation. Because of IC package limitations, the output dissipation is a total of 2.4 Watts for channels 1 to 8 and 2.4 Watts for channels 9 to 16.

If a single output is being used then the maximum permissible dissipation is 1.0 Watt. The absolute maximum permissible collector voltage is 50 volts.

CHAPTER 3

Programming Details

The address maps for DIO-32d is shown below. The card occupies a total of 8 contiguous addresses some of which are both read and write.

ADDRESS	FUNCTION	READ/ WRITE
Base + 0	Timer 0 input/output Register	R/W
Base + 1	Timer 1 input/output Register	R/W
Base + 2	Timer 2 input/output Register	R/W
Base + 3	Timer Control Register	W
Base + 4	Channels 1 To 8 Input	R
Base + 5	Channels 9 To 16 Input	R
Base + 6	Channels 1 To 8 Output	W
Base + 7	Channels 9 To 16 Output	W

µPD71054 Timer

The card utilises an NEC µPD71054 TIMER chip. This is equivalent to an Intel i8254 device. For full details on how to program the µPD71054 refer to the manufacturers' data sheets.

The µPD71054 contains three independent 16 bit counters which may be operated in various modes. Presented here is a brief summary of some of the modes possible by programming the timers' internal registers.

There are five basic modes of operation each providing a different output from the device. Timers 0 and 1 are connected in series to provide a longer delay period. Timer 2 in independent. The output from Timer 1 and Timer 2 are selectable by jumper to allow interrupt generation. The clock source for Timer 2 is link selectable.

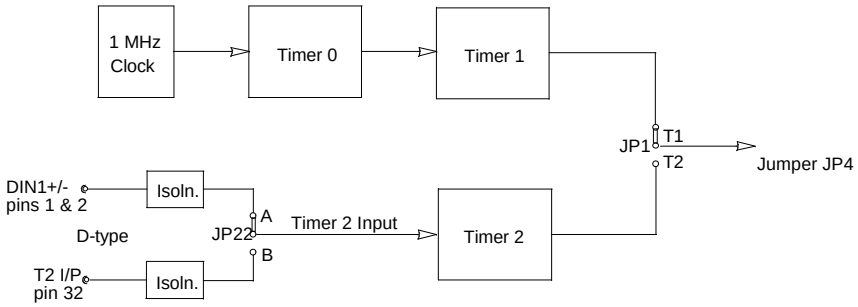


Figure 7 Timer Circuit Block Diagram

Timer Modes

The following modes of operation are possible by programming the control register within the µPD71054.

Mode 0

When programmed, the output pin will go LOW. When the counter decrements from the value loaded into the count registers to zero, the output pin will go HIGH. It will remain high until the count is re-programmed into the count registers.

Mode 1

Not Implemented

Mode 2

This mode operates as a frequency divider. When programmed, the output pin is high. When the count decrements to a value of 1 the output pin will go LOW for ONE clock cycle only and then return HIGH. This cycle repeats continuously without the need to re-program the count value.

Mode 3

The output pin toggles each time the count register decrements to its base level from the value programmed into it. If the count value loaded is an odd number then the counter will reach zero before the output pin toggles.

This mode acts as a frequency divider with an approximate 1:1 mark-space ratio.

Mode 4

This mode is similar to mode 2 but the output pin pulses when the count reaches zero instead of 1.

Mode 5

Not Implemented.

CHAPTER 4

Technical Specifications

Number of Input Channels	16
Number of Output Channels	16
Interrupt Signal Options	IRQ-2 to -7 inclusive

Input Characteristics

All Inputs Opto-Isolated from Computer Ground

Isolation Voltage	100 Volts
Voltage Input Range	Min. 3Volts
	Max. 24 Volts
Input Load Current	10ma @ 24v Input

Output Characteristics

All outputs are Opto-Isolated from Computer Ground

Isolation	100 volts
Output Type	Open Collector
Voltage Limits for each output	Min. 3 volts
	Max. 50 volts
Maximum Current Drive for each output	500mA
Maximum Total Load Power for each Block of 8 Outputs	4.8 Watts

Timers

Number of Timer Channels	3
Timer 0 And 1 (On-board Clock Source)	
Timer Resolution	1us
Min. Time Interval	1us
Max. Time Interval	65.535ms
Timer 2 (External Closk)	
Minimum Resolution	125ns
Min. Time Interval	125ns
Max. Time Interval Limited	None

Addresses

Total Addresses Required	8 (5 Read, 6 Write)

Board Connections

Input/Output	1 X 50 Way Male “D” Type
Bus	PC 8-bit ISA

Dimensions

	Board	**Overall**
Length	165	179
Height	107	127
Width	12	25

Electromagnetic Compatibility (EMC)

This product meets the requirements of the European EMC Directive (89/336/EEC) and is eligible to bear the CE mark.

It has been assessed operating in a Blue Chip Technology Icon industrial PC. However, because the board can be installed in a variety of computers, certain conditions have to be applied to ensure that the compatibility is maintained. It meets the requirements for an industrial environment (Class A product) subject to those conditions.

- The board must be installed in a computer system which provides screening suitable for the industrial environment.

- Any recommendations made by the computer system manufacturer/supplier must be complied with regarding earthing and the installation of boards.

- The board must be installed with the backplate securely screwed to the chassis of the computer to ensure good metal-to-metal (i.e. earth) contact.

- Most EMC problems are caused by the external cabling to boards. With analogue boards particular attention must be paid to this aspect. It is imperative that any external cabling to the board is totally screened, and that the screen of the cable connects to the metal end bracket of the board and hence to earth. It is recommended that round screened cables with a braided wire screen are used in preference to those with a foil screen and drain wire. Use metal connector shells which connect around the full circumference of the screen; they are far superior to those which earth the screen by a simple "pig-tail". Standard ribbon cable will not be adequate unless it is contained wholly within the cabinetry housing the industrial PC.

- To ensure that the board meets the industrial radiated field immunity of 10 V/metre, the cable should also be fitted with a ferrite clamp on the external cable as close as possible to the connector. The preferred type is the Chomerics clip-on style, type H8FE-1004-AS.

- Ensure that the screen of the external cable is bonded to a good RF earth at the remote end of the cable.

- Cables which connect externally to boards at TTL levels should not exceed two meters in length. This restriction does not apply to opto-isolated boards.

Failure to observe these recommendations may invalidate the EMC compliance.

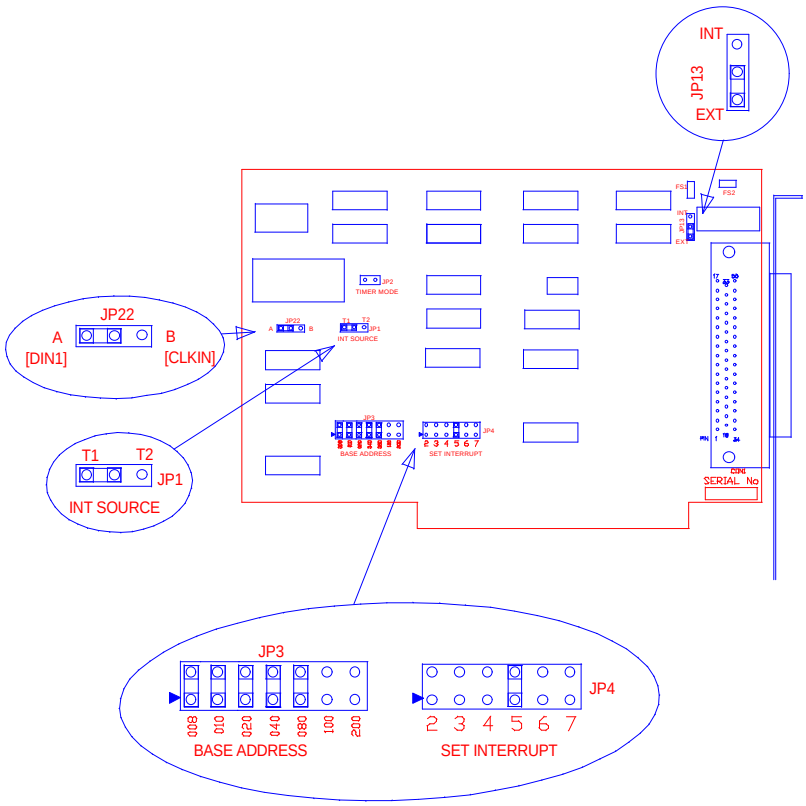
> Warning
> This is a Class A product. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

EMC Specification

A Blue Chip Technology Icon industrial PC fitted with this card meets the following specification:

Emissions:	EN 55022:1995	
	Radiated	Class A
	Conducted	Class A & B
Immunity:	pr EN 50082-2:1991 incorporating	
	Electrostatic Discharge	IEC 801-2:1984 Performance Criteria A
	Radio Frequency Susceptibility	IEC 801-3:1984 Performance Criteria A
	Fast Burst Transients	IEC 801-4:1988 Performance Criteria A

CARD LAYOUT


INT
JP13
EXT
JP22
A
[DIN1]
B
[CLKIN]
T1
T2
JP1
INT SOURCE
JP3
008
010
020
040
080
100
200
BASE ADDRESS
JP4
2 3 4 5 6 7
SET INTERRUPT
SERIAL No

APPENDIX A - NUMBERING SYSTEMS

Binary and Hexadecimal Numbers

The normal numbering system is termed DECIMAL because there are ten possible digits (0 to 9) in any single column of numbers. Decimal numbers are also referred to as numbers having a Base 10. When counting, the numbers increment in the units column from 0 up to 9. The next increment resets the units column to 0 and carries over 1 into the next column. This 1 indicates that there has been a full ten (the base number) counts in the units column. The second column is therefore termed the “tens” column.

It is more convenient when programming to use a number system that provides a clearer picture of the hardware at an operational or register level. The two most common number systems are used are BINARY and HEXADECIMAL. These two systems provide an alternative representation to decimal numbers.

For a binary number there are only 2 possible values (0 or 1) and as a result binary numbering is often known as Base 2. When counting in binary numbers the number increments the units column from 0 to 1. At the next increment the units column is reset to 0 and 1 is carried over to the next column. This column indicates that a full two counts have occurred in the units column. Now the second column is termed the “twos” column.

Hexadecimal numbers may have 16 values (0 to 9 followed by the letters A to F). It is also known as a system with the Base 16. With this counting system the units increment from 0 to 9 as with the decimal system, but at the next count the units column increments from 9 to A and then B, C and so on up to F. After F the units column resets to 0 and the next column increments from 0 to 1. This 1 indicates that sixteen counts have occurred in the units column. The second column is termed the “sixteen’s” column.

The following table shows how the three systems indicate successive numbers:

Decimal Base 10		Binary Base 2					Hexadecimal Base 16	
0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	1	0	1
0	2	0	0	0	1	0	0	2
0	3	0	0	0	1	1	0	3
0	4	0	0	1	0	0	0	4
0	5	0	0	1	0	1	0	5
0	6	0	0	1	1	0	0	6
0	7	0	0	1	1	1	0	7
0	8	0	1	0	0	0	0	8
0	9	0	1	0	0	1	0	9
1	0	0	1	0	1	0	0	A
1	1	0	1	0	1	1	0	B
1	2	0	1	1	0	0	0	C
1	3	0	1	1	0	1	0	D
1	4	0	1	1	1	0	0	E
1	5	0	1	1	1	1	0	F
1	6	1	0	0	0	0	1	0
1	7	1	0	0	0	1	1	1
1	8	1	0	0	1	0	1	2
1	9	1	0	0	1	1	1	3
2	0	1	0	1	0	0	1	4

Notice how the next higher column does not increment until the lesser one to its right has overflowed.

Binary representation is ideally suited where a visual representation of a computer register or data is needed. Each column is termed a BIT (from **B**inary dig**IT**). Only five Bits are shown in the above table. With larger numbers, more Bits are required. Normally Bits are arranged in groups of eight termed BYTES. By definition there are 8 BITS per BYTE. Each Bit (or column) has a value. In the binary table above the rightmost or least significant column each digit has a value of 1. Each digit in the next column has a value of 2, the next 4, then 8 and so on.

The following diagram illustrates this.

BIT No	7	6	5	4	3	2	1	0
DECIMAL VALUE	128	64	32	16	8	4	2	1

To determine the decimal value of a binary pattern, add up the decimal number of each column containing a binary "1".

BIT No	7	6	5	4	3	2	1	0
DECIMAL VALUE	128	64	32	16	8	4	2	1
BINARY NUMBER	1	1	0	0	0	1	1	0

The above example shows the binary pattern that is equivalent to 198 $_{Decimal}$.

The binary string defining a Byte can be unwieldy. To make it less error prone, the 8 bits forming a byte are divided into two groups of 4 bits, known as NIBBLES. With four bits there are 16 possible numeric combinations (including zero). A convenient method of representing each nibble is to use the hexadecimal base 16 system.

When converting binary to hex, the byte is divided into nibbles each represented by a single hex digit. This technique is applied to the selection of the base address for the circuit board. The following diagram illustrates the construction of a hex number.

BIT No	7	6	5	4	3	2	1	0
NIBBLE VALUE	8	4	2	1	8	4	2	1
BINARY NUMBER	1	1	0	0	0	1	1	0

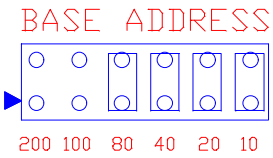
HEXADECIMAL: C 6

Hexadecimal upper nibble = (1 x 8) + (1 x 4) + (0 x 2) + (0 x 1) = 12
lower nibble = (0 x 8) + (1 x 4) + (1 x 2) + (0 x 1) = 6

The resulting value is C6 $_{Hex}$, since 12 $_{Decimal}$ equals C $_{Hex}$.

Base Address Selection

Each column can be physically represented on the board by a pair of pins. In practice, the boards cover a range of addresses (usually $16_{Decimal}$). Therefore the low order four bits are not included, but two higher order bits are added. This gives an address range of 0 to $3F0_{Hex}$. The following diagram shows a typical set of pins.



Here a link is fitted to denote a binary or logic “0”, or left open to indicate a binary or logic “1”. The example shows a base address setting of 300_{Hex}.

APPENDIX B - PC MAPS

PC/XT/AT I/O Address Map

Address	Allocated to:
000-01F	DMA Controller 1 (8237A-5)
020-03F	Interrupt Controller 1 (8259A)
040-05F	Timer (8254)
060-06F	Keyboard Controller (8742) Control Port B
070-07F	RTC and CMOS RAM, NMI Mask (Write)
080-09F	DMA Page Register (Memory Mapper)
0A0-0BF	Interrupt Controller 2 (8259)
0F0	Clear NPX (80287) Busy
0F1	Reset NPX (80287)
0F8-0FF	Numeric Processor Extension (80287)
1F0-1F8	Hard Disk Drive Controller
200-207	Reserved
278-27F	Reserved for Parallel Printer Port 2
2F8-2FF	Reserved for Serial Port 2
300-31F	Reserved
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	Reserved for SDLC Communications, Bisync 2
3A0-3AF	Reserved for Bisync 1
3B0-3BF	Reserved
3C0-3CF	Reserved
3D0-3DF	Display Controller
3F0-3F7	Diskette Drive Controller
3F8-3FF	Serial Port 1

PC/XT Interrupt Map

Number	Allocated to:
NMI	Parity
0	Timer
1	Keyboard
2	Reserved
3	Asynchronous Communications (Secondary) SDLC Communications
4	Asynchronous Communications (Primary) SDLC Communications
5	Fixed Disk
6	Diskette
7	Parallel Printer

PC/AT Interrupt Map

Level		Allocated to:
CPU NMI		Parity or I/O Channel Check
CTLR 1	CTLR 2	(Interrupt Controllers)
IRQ 0		Timer Output 0
IRQ 1		Keyboard (Output Buffer Full)
IRQ 2		Interrupt from CTLR 2
	IRQ 8	Real-time Clock Interrupt
	IRQ 9	S/w Redirected to INT 0AH (IRQ 2)
	IRQ 10	Reserved
	IRQ 11	Reserved
	IRQ 12	Reserved
	IRQ 13	Co-processor
	IRQ 14	Fixed Disk Controller
	IRQ 15	Reserved
IRQ 3		Serial Port 2
IRQ 4		Serial Port 1
IRQ 5		Parallel Port 2
IRQ 6		Diskette Controller
IRQ 7		Parallel Port 1

DMA Channels

0	Memory Refresh
1	Spare
2	Floppy Disk Drive
3	Spare